PCI EXPRESS®

GRAPHICS-CLASS

BACKPLANES

(PICMG® 1.3)

No. 87-006706-000 Revision i-G

TECHNICAL REFERENCE

WARRANTY

The following is an abbreviated version of Trenton Technology's warranty policy for PICMG® 1.3 products. For a complete warranty statement, contact Trenton or visit our website at www.TrentonTechnology.com.

Trenton PICMG® 1.3 products are warranted against material and manufacturing defects for five years from date of delivery to the original purchaser. Buyer agrees that if this product proves defective Trenton Technology Inc. is only obligated to repair, replace or refund the purchase price of this product at Trenton Technology's discretion. The warranty is void if the product has been subjected to alteration, neglect, misuse or abuse; if any repairs have been attempted by anyone other than Trenton Technology Inc.; or if failure is caused by accident, acts of God, or other causes beyond the control of Trenton Technology Inc. Trenton Technology Inc. reserves the right to make changes or improvements in any product without incurring any obligation to similarly alter products previously purchased.

In no event shall Trenton Technology Inc. be liable for any defect in hardware or software or loss or inadequacy of data of any kind, or for any direct, indirect, incidental or consequential damages arising out of or in connection with the performance or use of the product or information provided. Trenton Technology Inc.'s liability shall in no event exceed the purchase price of the product purchased hereunder. The foregoing limitation of liability shall be equally applicable to any service provided by Trenton Technology Inc.

RETURN POLICY

Products returned for repair must be accompanied by a Return Material Authorization (RMA) number, obtained from Trenton Technology prior to return. Freight on all returned items must be prepaid by the customer, and the customer is responsible for any loss or damage caused by common carrier in transit. Items will be returned from Trenton Technology via Ground, unless prior arrangements are made by the customer for an alternative shipping method

To obtain an RMA number, call us at (800) 875-6031 or (770) 287-3100. We will need the following information:

Return company address and contact
Model name and model # from the label on the back of the product
Serial number from the label on the back of the product
Description of the failure

An RMA number will be issued. Mark the RMA number clearly on the outside of each box, include a failure report for each board and return the product(s) to our Utica, NY facility:

TRENTON Technology Inc.
1001 Broad Street
Utica, NY 13501
Attn: Repair Department

Contact Trenton for our complete service and repair policy.

TRADEMARKS

LIABILITY DISCLAIMER

This manual is as complete and factual as possible at the time of printing; however, the information in this manual may have been updated since that time. Trenton Technology Inc. reserves the right to change the functions, features or specifications of their products at any time, without notice.

E-mail: Support@TrentonTechnology.com
Web: www.TrentonTechnology.com

TRENTON Technology Inc.
2350 Centennial Drive • Gainesville, Georgia 30504
Sales: (800) 875-6031 • Phone: (770) 287-3100 • Fax: (770) 287-3150

Table of Contents

HANDLING PRECAUTIONS

WARNING: This product has components which may be damaged by electrostatic discharge.

To protect your backplane from electrostatic damage, be sure to observe the following precautions when handling or storing the backplane:

- Keep the backplane in its static-shielded bag until you are ready to perform your installation.
- Handle the backplane by its edges.
- Do not touch the I/O connector pins. Do not apply pressure or attach labels to the backplane.
- Use a grounded wrist strap at your workstation or ground yourself frequently by touching the metal chassis of the system before handling any components. The system must be plugged into an outlet that is connected to an earth ground.
- Use antistatic padding on all work surfaces.
- Avoid static-inducing carpeted areas.

Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your Trenton PCI Express® backplane. Overall system performance may be affected by incorrect usage of these features.

PCI EXPRESS® LINKS

PCI Express devices with different PCI Express link configurations can establish communication using a process called auto-negotiation or link training. If a board with a higher number of lanes is placed in a slot with a lower number of lanes (e.g., a x16 board in a x16 mechanical slot electrically configured with a x4 PCIe link) or a board with a lower number of lanes is placed into a slot with a higher number of lanes (e.g., a x4 board into a x8 slot), the PCI Express link auto-negotiates down to the lower link rate to establish communication to the system host board (SHB). The mechanical option card slots on Trenton PICMG® 1.3 backplanes have PCI Express configuration straps. Some SHB designs may utilize the straps in the PCI Express link width negotiation process.

SHB AND PICMG® 1.3 BACKPLANE CONFIGURATIONS

Trenton's BPG4 (6537-xxx), BPG2/2 (6532-xxx), BPG6544 (6544-xxx) and BPG6600 (6600- xxx), BPG6615 (6615- xxx), BPG6714 (6714- xxx) and BPG6741 (6741- xxx) backplanes support a graphics-class configuration of the PCI Express links. In this type of configuration, the SHB supports one x16 PCI Express link and a single x4 link to the graphics-class backplane. These backplanes also support an additional x1 link when using Trenton's IOB31 I/O expansion board on a Trenton graphics-class SHB. The letter "G" in a Trenton backplane model name indicates a graphics-class configuration.

NOTE: Graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes and server-class SHBs should always be used with server-class PICMG 1.3 backplanes. Combining incompatible SHBs and backplanes will not cause damage to the option cards or SHB, but one or more of the slots may not function and may result in one or more PCI Express option cards on the backplane being non-functional. This is due to the fact that there may not be enough available links to properly connect all of the PCI Express option card slots to the SHB.

OPTIONAL I/O CONNECTIONS

The PICMG 1.3 specification enables SHB vendors to route I/O connections to edge connector C of an SHB. Trenton PICMG 1.3 backplanes support the four USB and two Ethernet connections, but since these connections are optional, not all SHBs support them. In order to take advantage of these I/O features, the SHB in your system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

POWER CONNECTION

Trenton's PCI Express backplanes support soft power control signals via the Advanced Configuration and Power Interface (ACPI) as defined in the PICMG 1.3 specification. When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

+12V AUXILIARY POWER CONNECTION

Trenton PICMG 1.3 backplanes provide one or more +12V power connectors for routing auxiliary power to the SHB's edge connectors, eliminating the need for auxiliary power connections on the system host board. These are 8-pin connectors that can accommodate either a 4-pin or 8-pin power cable connection.

POWER CAUTIONS

CAUTION: Trenton recommends using EPS model power supplies with its PICMG 1.3 backplanes in systems using high-performance, dual-processor SHB Express system host boards.

The power needs of backplane option cards, high-performance processors and other system components may result in drawing 20A of current from the +12V power supply line. If this occurs, hazardous energy (240VA) could exist inside the system chassis. Final system/equipment suppliers must provide protection to service personnel from these potentially hazardous energy levels.

Standby voltages may be used in the final system design to enable certain system recovery operations. In this case, the power supply may not completely remove power to the system host board when the power switch is turned off. Caution must be taken to ensure that incoming system power is completely disconnected before removing the system host board.

In some ATX/EPS systems, the power may appear to be off while the 5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the 5VSB power signal; "green" indicates that the 5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

BACKPLANE HOLE PATTERNS

The PICMG 1.3 specification defines recommended backplane sizes and hole patterns. These hole patterns are not the same as motherboard hole patterns. Trenton's backplanes support Trenton's hole patterns for 14-slot (64-bit) and 20-slot (64-bit) backplanes as well as the hole patterns specified for PICMG 1.3 backplanes. The Trenton 14-slot hole pattern on the BPX3/8 backplane is modified slightly to accommodate the backplane's smaller width dimension. The backplane chapters in the *PCI Express® Graphics-class Backplanes Manual* contains mechanical dimensions and hole patterns for individual Trenton PCI Express backplanes.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections of the *PCI Express® Backplanes Technical Reference Manual* (#87-006706-000). The latest revision of this manual may be found on Trenton's website - www.TrentonTechnology.com.

This page intentionally left blank.

Chapter 1 - Backplane Overview

INTRODUCTION

Trenton PCI Express® graphics-class backplanes are six-layer or eight-layer backplanes which are PICMG® 1.3 compatible and allow the use of standard PCI Express, PCI-X, PCI or ISA option cards. Types and numbers of option cards supported vary depending on the backplane model.

Each backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). The backplanes have a varying number of PCI Express slots available for use.

NOTE: On some of the backplanes, one of the PCI Express slots connects to a PCI Express expansion slot (PCIeS) on the backplane. In order to use this PCIe slot when you are using a Trenton PCI Express SHB, you must have a Trenton IOB31 (6474-000) I/O expansion board on the SHB. The IOB31 enables communication between the SHB and the PCI Express slot by providing a x1 or x4 PCI Express link to the PCIeS slot, depending on the capabilities of the SHB.

Refer to the backplane descriptions in the following chapters of this manual for more information about a specific backplane.

MODELS

NOTE: In the chart below, the descriptions of the PCI Express slots include the electrical link rate of the slots, not the mechanical size.

Model #	Model Name	Description
Graphics-Class Backplanes:		
6532-000	BPG2/2	1 SHB Slot, 1 x16 PCI Express, 2 PCI-X 64-bit/133MHz
6537-000	BPG4	1 SHB Slot, 1 x16 PCI Express, 1 x4 PCI Express, 1 x1 PCI Express via a PCIe Expansion Slot
6544-000	BPG6544	1 SHB Slot, 1 x16 PCI Express, 1 z4/x1 PCI Express via a PCIe Expansion Slot, 1 PCI-X 64-bit/133MHz, 4 PCI-X 64-bit/66MHz, 2 PCI 32-bit/33MHz, 2 ISA 32-bit/33MHz

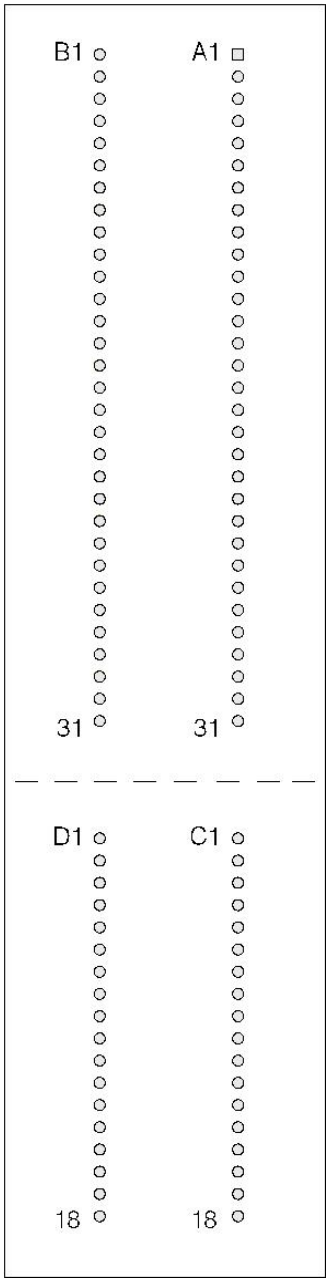
Model #	Model Name	Description
Graphics-Class Backplanes: (Continued)		
6600-000	BPG6600	1 SHB Slot, 1 x16 PCI Express, 1 x4/x1 PCI Express via a PCIe Expansion Slot, 2 PCI-X 64-bit/100MHz, 4 PCI-X 64-bit/66MHz, 4 PCI 32-bit/33MHz
6615-000	BPG6615	1 SHB Slot, 1 x16 PCI Express, 4 x4 PCI Express, 2 PCI-X 64-bit/100MHz, 4 PCI-X 64-bit/66MHz
6714-000	BPG6714	1 SHB Slot, 1 x16 PCI Express, 1 x4 PCI Express, 1 x4/x1 PCI Express via a PCIe Expansion Slot, 1 PCI-X 64-bit/133MHz, 2 PCI-X 64-bit/100MHz
Mutilple SHB-Class Backplanes		
6605-000	BP6FS6605	6 SHB Slot, 6 x16 PCI Express, 3 x4 PCI Express
2U Butterfly-Class Backplanes		
6741-000	BPG6741	1 SHB Slot, 1 x16 PCI Express, 2 x1 PCI Express

FEATURES

- Six-layer or eight-layer printed circuit board
- High noise immunity construction
- Accept system host boards (SHBs) which are PCI Industrial Computer Manufacturers Group (PICMG®) 1.3 compatible
- Allow use of standard PCI Express, PCI-X, PCI or ISA option cards, depending on model
- Multiple power supply connectors, depending on model

Chapter 2 - ISA/PCI Reference

ISA BUS PIN NUMBERING



62-pin ISA Bus Connector

Component Side of Board

36-pin ISA Bus Connector

ISA BUS PIN ASSIGNMENTS

The following tables summarize pin assignments for the Industry Standard Architecture (ISA) Bus connectors.

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
A1	IOCHK#	I	B1	Gnd	Ground
A2	D7	I/O	B2	RESDRV	O
A3	D6	I/O	B3	+5V	Power
A4	D5	I/O	B4	IRQ9	I
A5	D4	I/O	B5	-5V	Power
A6	D3	I/O	B6	DRQ2	I
A7	D2	I/O	B7	-12V	Power
A8	D1	I/O	B8	NOWS#	I
A9	D0	I/O	B9	+12V	Power
A10	CHRDY	I	B10	Gnd	Ground
A11	AEN	O	B11	SMWTC#	O
A12	SA19	I/O	B12	SMRDC#	O
A13	SA18	I/O	B13	IOWC#	I/O
A14	SA17	I/O	B14	IORC#	I/O
A15	SA16	I/O	B15	DAK3#	O
A16	SA15	I/O	B16	DRQ3	I
A17	SA14	I/O	B17	DAK1#	O
A18	SA13	I/O	B18	DRQ1	I
A19	SA12	I/O	B19	REFRESH#	I/O
A20	SA11	I/O	B20	BCLK	O
A21	SA10	I/O	B21	IRQ7	I
A22	SA9	I/O	B22	IRQ6	I
A23	SA8	I/O	B23	IRQ5	I
A24	SA7	I/O	B24	IRQ4	I
A25	SA6	I/O	B25	IRQ3	I
A26	SA5	I/O	B26	DAK2#	O
A27	SA4	I/O	B27	T-C	O
A28	SA3	I/O	B28	BALE	O
A29	SA2	I/O	B29	+5V	Power
A30	SA1	I/O	B30	OSC	O
A31	SA0	I/O	B31	Gnd	Ground

I/O Pin	Signal Name	I/O	I/O Pin	Signal Name	I/O
C1	SBHE#	I/O	D1	M16#	I
C2	LA23	I/O	D2	IO16#	I
C3	LA22	I/O	D3	IRQ10	I
C4	LA21	I/O	D4	IRQ11	I
C5	LA20	I/O	D5	IRQ12	I
C6	LA19	I/O	D6	IRQ15	I
C7	LA18	I/O	D7	IRQ14	I
C8	LA17	I/O	D8	DAK0#	O
C9	MRDC#	I/O	D9	DRQ0	I
C10	MWTC#	I/O	D10	DAK5#	O
C11	D8	I/O	D11	DRQ5	I
C12	D9	I/O	D12	DAK6#	O
C13	D10	I/O	D13	DRQ6	I
C14	D11	I/O	D14	DAK7#	O
C15	D12	I/O	D15	DRQ7	I
C16	D13	I/O	D16	+5V	Power
C17	D14	I/O	D17	Master16#	I
C18	D15	I/O	D18	Gnd	Ground

ISA BUS SIGNAL DESCRIPTIONS

The following is a description of the ISA Bus signals. All signal lines are TTL- compatible.

AEN (O)

Address Enable (AEN) is used to degate the microprocessor and other devices from the I/O channel to allow DMA transfers to take place. When this line is active, the DMA controller has control of the address bus, the data-bus Read command lines (memory and I/O), and the Write command lines (memory and I/O).

BALE (O) (Buffered)

Address Latch Enable (BALE) is provided by the bus controller and is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the I/O channel as an indicator of a valid microprocessor or DMA address (when used with AEN). Microprocessor addresses SA[19::0] are latched with the falling edge of BALE. BALE is forced high during DMA cycles.

BCLK (O)

BCLK is the system clock. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for uses requiring a fixed frequency.

CHRDY (I)

I/O Channel Ready (CHRDY) is pulled low (not ready) by a memory or I/O device to lengthen I/ O or memory cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read or Write command. Machine cycles are extended by an integral number of clock cycles. This signal should be held low for no more than 2.5 microseconds.

D[15::0] (I/O)

Data signals D[15::0] provide bus bits 15 through 0 for the microprocessor, memory, and I/O devices. D15 is the most-significant bit and D0 is the least-significant bit. All 8-bit devices on the I/O channel should use D[7::0] for communications to the microprocessor. The 16-bit devices will use D[15::0]. To support 8-bit devices, the data on D[15::8] will be gated to D[7::0] during 8-bit transfers to these devices. 16-bit microprocessor transfers to 8-bit devices will be converted to two 8-bit transfers.

DAK[7::5]#, DAK[3::0]# (O)

DMA Acknowledge DAK[7::5]# and DAK[3::0]# are used to acknowledge DMA requests DRQ[7::5] and DRQ[3::0]. They are active low.

DRQ[7::5], DRQ[3::0] (I)

DMA Requests DRQ[7::5] and DRQ[3::0] are asynchronous channel requests used by peripheral devices and the I/O channel microprocessors to gain DMA service (or control of the system). They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DAK) line goes active. DRQ[3::0] will perform 8-bit DMA transfers; DRQ[7::5] will perform 16-bit transfers.

IO16# (I)

I/O 16-bit Chip Select (IO16#) signals the system board that the present data transfer is a 16-bit, 1 wait-state, I/O cycle. It is derived from an address decode. IO16# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

IOCHK# (I)

I/O Channel Check (IOCHK#) provides the system board with parity (error) information about memory or devices on the I/O channel. When this signal is active, it indicates an uncorrectable system error.

IORC# (I/O)

I/O Read (IORC#) instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor or DMA controller, or by a microprocessor or DMA controller resident on the I/O channel. This signal is active low.

IOWC# (I/O)

I/O Write (IOWC#) instructs an I/O device to read the data on the data bus. It may be driven by any microprocessor or DMA controller in the system. This signal is active low.

IRQ[15::14], IRQ[12::9], IRQ[7::3] (I)

Interrupt Requests IRQ[15::14], IRQ[12::9] and IRQ[7::3] are used to signal the microprocessor that an I/O device needs attention. The interrupt requests are prioritized, with IRQ[15::14] and IRQ[12::9] having the highest priority (IRQ9 is the highest) and IRQ[7::3] having the lowest priority (IRQ7 is the lowest). An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request (Interrupt Service routine).

LA[23::17] (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. They give the system up to 16MB of addressability. These signals are valid when BALE is high. LA[23::17] are not latched during microprocessor cycles and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for 1 wait-state memory cycles. These decodes should be latched by I/O adapters on the falling edge of BALE. These signals also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

M16# (I)

M16# Chip Select signals the system board if the present data transfer is a 1<N>wait-state, 16- bit, memory cycle. It must be derived from the decode of LA[23::17]. M16# should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

Master16# (I)

Master16# is used with a DRQ line to gain control of the system. A processor or DMA controller on the I/O channel may issue a DRQ to a DMA channel in cascade mode and receive a DAK#. Upon receiving the DAK#, an I/O microprocessor may pull Master16# low, which will allow it to control the system address, data, and control lines (a condition known as tri-state). After Master16# is low, the I/O microprocessor must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15<N>microseconds, system memory may be lost because of a lack of refresh.

NOWS# (I)

The No Wait State (NOWS#) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. In order to run a memory cycle to a 16-bit device without wait cycles, NOWS# is derived from an address decode gated with a Read or Write command. In order to run a memory cycle to an 8-bit device with a minimum of two wait states, NOWS# should be driven active on system clock after the Read or Write command is active gated with the address decode for the device. Memory Read and Write commands to a 8-bit device are active on the falling edge of the system clock. NOWS# is active low and should be driven with an open collector or tri-state driver capable of sinking 20 mAmps.

OSC (O)

Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

REFRESH# (I/O)

The REFRESH# signal is used to indicate a refresh cycle and can be driven by a microprocessor on the I/O channel.

RESDRV (O)

Reset Drive (RESDRV) is used to reset or initialize system logic at power-up time or during a low line-voltage outage. This signal is active high.

SA[19::0] (I/O)

Address bits SA[19::0] are used to address memory and I/O devices within the system. These twenty address lines, in addition to LA[23::17], allow access of up to 16MB of memory. SA[19::0] are gated on the system bus when BALE is high and are latched on the falling edge of BALE. These signals are generated by the microprocessor or DMA Controller. They also may be driven by other microprocessors or DMA controllers that reside on the I/O channel.

SBHE# (I/O)

System Bus High Enable (SBHE#) indicates a transfer of data on the upper byte of the data bus, D[15::8]. 16-bit devices use SBHE# to condition data bus buffers tied to D[15::8].

SMRDC# (O), MRDC# (I/O)

These signals instruct the memory devices to drive data onto the data bus. SMRDC# is active only when the memory decode is within the low 1MB of memory space. MRDC# is active on all memory read cycles. MRDC# may be driven by any microprocessor or DMA controller in the system. SMRDC is derived from MRDC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MRDC#, it must have the address lines valid on the bus for one system clock period before driving MRDC# active. Both signals are active low.

SMWTC# (O), MWTC# (I/O)

These signals instruct the memory devices to store the data present on the data bus. SMWTC# is active only when the memory decode is within the low 1MB of the memory space. MWTC# is active on all memory write cycles. MWTC# may be driven by any microprocessor or DMA controller in the system. SMWTC# is derived from MWTC# and the decode of the low 1MB of memory. When a microprocessor on the I/O channel wishes to drive MWTC#, it must have the address lines valid on the bus for one system clock period before driving MWTC# active. Both signals are active low.

T-C (O)

Terminal Count (T-C) provides a pulse when the terminal count for any DMA channel is reached.

I/O ADDRESS MAP*

Hex Range	Device
000-01F	DMA Controller 1
020-03F	Interrupt Controller 1, Master
040-05F	Timer
060-06F	8042 (Keyboard)
070-07F	Real-time Clock, NMI (non-maskable interrupt) Mask
080-09F	DMA Page Register
0A0-0BF	Interrupt Controller 2
0C0-0DF	DMA Controller 2
0F0	Clear Math Coprocessor Busy
0F1	Reset Math Coprocessor
0F8-0FF	Math Coprocessor
1F0-1F8	Fixed Disk
200-207	Game I/O
278-27F	Parallel Printer Port 2
2F8-2FF	Serial Port 2
300-31F	Prototype Card
360-36F	Reserved
378-37F	Parallel Printer Port 1
380-38F	SDLC, Bisynchronous 2
3A0-3AF	Bisynchronous 1
3B0-3BF	Monochrome Display and Printer Adapter
3C0-3CF	Reserved
3D0-3DF	Color/Graphics Monitor Adapter
3F0-3F7	Diskette Controller
3F8-3FF	Serial Port 1

INTERRUPT ASSIGNMENTS*

Interrupt	Description
IRQ0	Timer Output 0
IRQ1	Keyboard (Output Buffer Full)
IRQ2	Interrupt 8 through 15
IRQ3	Serial Port 2
IRQ4	Serial Port 1
IRQ5	Parallel Port 2
IRQ6	Diskette Controller
IRQ7	Parallel Port 1
IRQ8	Real-time Clock Interrupt
IRQ9	Software Redirected to INT 0AH (IRQ2)
IRQ10	Unassigned
IRQ11	Unassigned
IRQ12	Unassigned
IRQ13	Coprocessor
IRQ14	Fixed Disk Controller
IRQ15	Unassigned

* These are typical parameters, which may not reflect your current system.

PCI LOCAL BUS OVERVIEW

The PCI (Peripheral Component Interconnect) Local Bus is a high performance, 32-bit or 64-bit bus with multiplexed address and data lines. It is intended for use as an interconnect mechanism between highly integrated peripheral controller components, peripheral add-in boards and processor/memory systems.

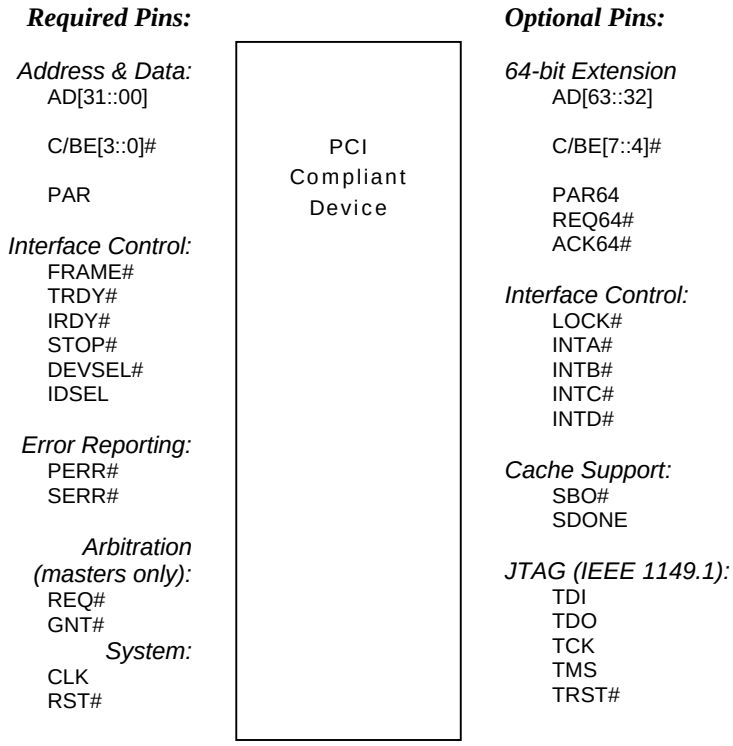
The "local bus" moves peripheral functions with high bandwidth requirements closer to the system's processor bus and can produce substantial performance gains with graphical user interfaces (GUIs) and other high bandwidth functions (i.e., full motion video, SCSI, LANs, etc.).

The PCI Local Bus accommodates future system requirements and is applicable across multiple platforms and architectures.

The PCI component and add-in card interface is processor independent, enabling an efficient transition to future processor generations, by bridges or by direct integration, and use with multiple processor architectures. Processor independence allows the PCI Local Bus to be optimized for I/O functions, enables concurrent operation of the local bus with the processor/memory subsystem, and accommodates multiple high performance peripherals in addition to graphics. Movement to enhanced video and multimedia displays and other high bandwidth I/O will continue to increase local bus bandwidth requirements. A transparent 64-bit extension of the 32-bit data and address buses is defined, doubling the bus bandwidth and offering forward and backward compatibility of 32-bit (132MB/s peak) and 64-bit (264MB/s peak) PCI Local Bus peripherals.

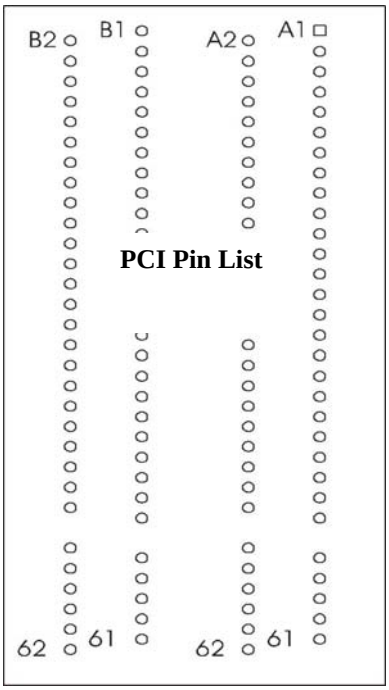
PCI LOCAL BUS SIGNAL DEFINITION

The PCI interface requires a minimum of 47 pins for a target-only device and 49 pins for a master to handle data and addressing, interface control, arbitration and system functions. The diagram below shows the pins in functional groups, with required pins on the left side and optional pins on the right side.



PCI LOCAL BUS PIN NUMBERING

Component Side of Board



5-volt/32-bit PCI Connector

PCI LOCAL BUS PIN ASSIGNMENTS

The PCI Local Bus pin assignments shown below are for the PCI option slots on the backplane.

The PCI Local Bus specifies both 5-volt and 3.3-volt signaling environments. The following bus pin assignments are for the 5-volt connector. The 3.3-volt connector bus pin assignments are the same with the following exceptions:

* The pins noted as +V (I/O) are +5 volts or +3.3 volts, depending on which connector is being used.

† Pins B12, B13, A12 and A13 are Gnd (ground) on the 5-volt connector, but are Connector Keys on the 3.3-volt connector.

†† Pin B49 is Gnd (ground) on the 5-volt connector, but is M66EN on the 3.3- volt connector.

††† Pins B50, B51, A50 and A51 are Connectors Keys on the 5-volt connector, but are Gnd (ground) on the 3.3-volt connector.

I/O Pin	Signal Name		I/O Pin	Signal Name	
B1	-12V		A1	TRST#	32-bit connector
B2	TCK		A2	+12V	
B3	Gnd		A3	TMS	
B4	TDO		A4	TDI	
B5	+5V		A5	+5V	
B6	+5V		A6	INTA#	
B7	INTB#		A7	INTC#	
B8	INTD#		A8	+5V	
B9	PRSNT1#		A9	Reserved	
B10	Reserved		A10	+V (I/O) *	
B11	PRSNT2#		A11	Reserved	
B12	Gnd		A12	Gnd	3.3-Volt Key
B13	Gnd		A13	Gnd	3.3-Volt Key
B14	Reserved		A14	Reserved	
B15	Gnd		A15	RST#	
B16	CLK		A16	+V (I/O) *	
B17	Gnd		A17	GNT#	
B18	REQ#		A18	Gnd	
B19	+V (I/O) *		A19	Reserved	
B20	AD31		A20	AD30	
B21	AD29		A21	+3.3V	
B22	Gnd		A22	AD28	
B23	AD27		A23	AD26	
B24	AD25		A24	Gnd	
B25	+3.3V		A25	AD24	
B26	C/BE3#		A26	IDSEL	
B27	AD23		A27	+3.3V	
B28	Gnd		A28	AD22	
B29	AD21		A29	AD20	
B30	AD19		A30	Gnd	
B31	+3.3V		A31	AD18	
B32	AD17		A32	AD16	
B33	C/BE2#		A33	+3.3V	
B34	Gnd		A34	FRAME#	
B35	IRDY#		A35	Gnd	

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

I/O Pin	Signal Name	I/O Pin	Signal Name	
B36	+3.3V	A36	TRDY#	
B37	DEVSEL#	A37	Gnd	
B38	Gnd	A38	STOP#	
B39	LOCK#	A39	+3.3V	
B40	PERR#	A40	SDONE	
B41	+3.3V	A41	SBO#	
B42	SERR#	A42	Gnd	
B43	+3.3V	A43	PAR	
B44	C/BE1#	A44	AD15	
B45	AD14	A45	+3.3V	
B46	Gnd	A46	AD13	
B47	AD12	A47	AD11	
B48	AD10	A48	Gnd	
B49	Gnd	A49	AD9	
B50	Connector Key	A50	Connector Key	5-volt key
B51	Connector Key	A51	Connector Key	5-volt key
B52	AD8	A52	C/BE0#	
B53	AD7	A53	+3.3V	
B54	+3.3V	A54	AD6	
B55	AD5	A55	AD4	
B56	AD3	A56	Gnd	
B57	Gnd	A57	AD2	
B58	AD1	A58	AD0	
B59	+V (I/O) *	A59	+V (I/O) *	
B60	ACK64#	A60	REQ64#	
B61	+5V	A61	+5V	
B62	+5V	A62	+5V	32-bit connector end

PCI LOCAL BUS PIN ASSIGNMENTS (CONTINUED)

The following pin assignments apply only to backplanes with 64-bit PCI option slots.

I/O Pin	Signal Name	I/O Pin	Signal Name	
	Connector Key		Connector Key	64-bit spacer
	Connector Key		Connector Key	64-bit spacer
B63	Reserved	A63	Gnd	64-bit connector start
B64	Gnd	A64	C/BE7#	
B65	C/BE6#	A65	C/BE5#	
B66	C/BE4#	A66	+V (I/O) *	
B67	Gnd	A67	PAR64	
B68	AD63	A68	AD62	
B69	AD61	A69	Gnd	
B70	+V (I/O) *	A70	AD60	
B71	AD59	A71	AD58	
B72	AD57	A72	Gnd	
B73	Gnd	A73	AD56	
B74	AD55	A74	AD54	
B75	AD53	A75	+V (I/O) *	
B76	Gnd	A76	AD52	
B77	AD51	A77	AD50	
B78	AD49	A78	Gnd	
B79	+V (I/O) *	A79	AD48	
B80	AD47	A80	AD46	
B81	AD45	A81	Gnd	
B82	Gnd	A82	AD44	
B83	AD43	A83	AD42	
B84	AD41	A84	+V (I/O) *	
B85	Gnd	A85	AD40	
B86	AD39	A86	AD38	
B87	AD37	A87	Gnd	
B88	+V (I/O) *	A88	AD36	
B89	AD35	A89	AD34	
B90	AD33	A90	Gnd	
B91	Gnd	A91	AD32	
B92	Reserved	A92	Reserved	
B93	Reserved	A93	Gnd	
B94	Gnd	A94	Reserved	64-bit connector end

PCI LOCAL BUS SIGNAL DESCRIPTIONS

The PCI Local Bus signals are described below and may be categorized into the following functional groups:

- System Pins
- Address and Data Pins
- Interface Control Pins
- Arbitration Pins (Bus Masters Only)
- Error Reporting Pins
- Interrupt Pins (Optional)
- Cache Support Pins (Optional)
- 64-Bit Bus Extension Pins (Optional)
- JTAG/Boundary Scan Pins (Optional)

A # symbol at the end of a signal name indicates that the active state occurs when the signal is at a low voltage. When the # symbol is absent, the signal is active at a high voltage.

The following are descriptions of the PCI Local Bus signals.

ACK64# (optional)

Acknowledge 64-bit Transfer, when actively driven by the device that has positively decoded its address as the target of the current access, indicates the target is willing to transfer data using 64bits. ACK64# has the same timing as DEVSEL#.

AD[31::00]

Address and Data are multiplexed on the same PCI pins. A bus transaction consists of an address phase followed by one or more data phases. During the address phase, AD[31::00] contain a physical address (32 bits). During data phases, AD[07::00] contain the least significant byte (lsb) and AD[31::24] contain the most significant byte (msb).

AD[63::32] (optional)

Address and Data are multiplexed on the same pins and provide 32additional bits. During an address phase (when using the DAC command and when REQ64# is asserted), the upper 32bits of a 64-bit address are transferred; otherwise, these bits are reserved but are stable and indeterminate. During a data phase, an additional 32bits of data are transferred when REQ64# and ACK64# are both asserted.

C/BE[3::0]#

Bus Command and Byte Enables are multiplexed on the same PCI pins. During the address phase of a transaction, these pins define the bus command; during the data phase they are used as byte enables. The byte enables are valid for the entire data phase and determine which byte lanes carry meaningful data. C/BE0# applies to byte0 (lsb) and C/BE3# applies to byte 3 (msb).

C/BE[7::4]# (optional)

Bus Command and Byte Enables are multiplexed on the same pins. During an address phase (when using the DAC command and when REQ64# is asserted), the actual bus command is transferred on C/BE[7::4]#; otherwise, these bits are reserved and indeterminate. During a data phase, C/BE[7::4]# are byte enables indicating which byte lanes carry meaningful data when REQ64# and ACK64# are both asserted. C/BE4# applies to byte4 and C/BE7# applies to byte7.

CLK

Clock provides timing for all transactions on PCI and is an input to every PCI device.

DEVSEL#

Device Select, when actively driven, indicates that the driving device has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.

FRAME#

Cycle Frame is an interface control pin which is driven by the current master to indicate the beginning and duration of an access. When FRAME# is asserted, data transfers continue; when it is deasserted, the transaction is in the final data phase.

GNT#

Grant indicates to the agent that access to the bus has been granted. This is a point to point signal. Every master has its own GNT#.

IDSEL

Initialization Device Select is used as a chip select during configuration read and write transactions.

INTA#, INTB#, INTC#, INTD# (optional)

Interrupts on PCI are optional and defined as "level sensitive," asserted low (negative true), using open drain output drivers. PCI defines one interrupt for a single function and up to four interrupt lines for a multi-function device or connector.

Interrupt A is used to request an interrupt. For a single function device, only INTA# may be used, while the other three interrupt lines have no meaning.

Interrupt B, Interrupt C and Interrupt D are used to request additional interrupts and only have meaning on a multi-function device.

IRDY#

Initiator Ready indicates the initiating agent's (bus master's) ability to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. During a write, IRDY# indicates that valid data is present on AD[31::0]. During a read, it indicates that the master is prepared to accept data.

LOCK#

Lock indicates an operation that may require multiple transactions to complete. When LOCK# is asserted, non-exclusive transactions may proceed to an address that is not currently locked.

PAR

Parity is even parity across AD[31::00] and C/BE[3::0]#. Parity generation is required by all PCI agents. The master drives PAR for address and write data phases; the target drives PAR for read data phases.

PAR64 (optional)

Parity Upper DWORD is the even parity bit that protects AD[63::32] and C/BE[7::4]#. The master drives PAR64 for address and write data phases; the target drives PAR64 for read data phases.

PERR#

Parity Error is for the reporting of data parity errors during all PCI transactions except a Special Cycle. There are no special conditions when a data parity error may be lost or when reporting of an error may be delayed.

PRSNT1# and PRSNT2#

PRSNT1# and PRSNT2# are related to the connector only, not to other PCI components. They are used for two purposes: indicating that a board is physically present in the slot and providing information about the total power requirements of the board.

REQ#

Request indicates to the arbiter that this agent desires use of the bus. This is a point to point signal. Every master has its own REQ#.

REQ64# (optional)

Request 64-bit Transfer, when actively driven by the current bus master, indicates it desires to transfer data using 64 bits. REQ64# has the same timing as FRAME#. REQ64# has meaning at the end of reset.

RST#

Reset is used to bring PCI-specific registers, sequencers and signals to a consistent state.

SBO# (optional)

Snoop Backoff is an optional cache support pin which indicates a hit to a modified line when asserted. When SBO# is deasserted and SDONE is asserted, it indicates a "clean" snoop result.

SDONE (optional)

Snoop Done is an optional cache support pin which indicates the status of the snoop for the current access. When deasserted, it indicates the result of the snoop is still pending. When asserted, it indicates the snoop is complete.

SERR#

System Error is for reporting address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic. If an agent does not want a non-maskable interrupt (NMI) to be generated, a different reporting mechanism is required.

STOP#

Stop indicates that the current target is requesting the master to stop the current transaction.

TCK (optional)

Test Clock is used to clock state information and test data into and out of the device during operation of the TAP (Test Access Port).

TDI (optional)

Test Data Input is used to serially shift test data and test instructions into the device during TAP (Test Access Port) operation.

TDO (optional)

Test Data Output is used to serially shift test data and test instructions out of the device during TAP (Test Access Port) operation.

TMS (optional)

Test Mode Select is used to control the state of the TAP (Test Access Port) controller in the device.

TRDY#

Target Ready indicates the target agent's (selected device's) ability to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. During a read, TRDY# indicates that valid data is present on AD[31::00]. During a write, it indicates that the target is prepared to accept data.

TRST# (optional)

Test Reset provides an asynchronous initialization of the TAP controller. This signal is optional in the IEEE Standard Test Access Port and Boundary Scan Architecture.

This page intentionally left blank.

Chapter 3 - PCI Express® Reference

INTRODUCTION

PCI Express® is a high-speed, high-bandwidth interface with multiple channels (lanes) bundled together with each lane using full-duplex, serial data transfers with high clock frequencies.

The PCI Express architecture is based on the conventional PCI addressing model, but improves upon it by providing a high-performance physical interface and enhanced capabilities. Whereas the PCI bus architecture provided parallel communication between a processor board and backplane, the PCI Express protocol provides high-speed serial data transfer, which allows for higher clock speeds. The same data rate is available in both directions simultaneously, effectively reducing bottlenecks between the system host board (SHB) and PCI Express option cards.

PCI Express option cards may require updated device drivers. Most operating systems that support legacy PCI cards will also support PCI Express cards without modification. Because of this design, PCI, PCI-X and PCI Express option cards can co-exist in the same system.

PCI Express connectors have lower pin counts than PCI bus connectors. The PCIe connectors are physically different, based on the number of lanes in the connector.

PCI EXPRESS® LINKS

Several PCI Express channels (lanes) can be bundled for each expansion slot, leaving room for stages of expansion.

A basic PCI Express lane consists of a set of differential signal pairs: one pair for transmission and one pair for reception. A PCI Express link is a collection of one or more PCIe lanes. PCI Express supports scalable link widths in 1-, 4-, 8- and 16-lane configurations, generally referred to as x1, x4, x8 and x16 slots. A x1 ("by 1") slot indicates that the slot has one PCIe lane, which gives it a bandwidth of 250MB/s in each direction. Since devices do not compete for bandwidth, the effective bandwidth, counting bandwidth in both directions, is 500MB/s (full-duplex).

The number and configuration of an SHB's PCI Express links is determined by specific component PCI Express specifications. The bandwidths for the PCIe links are determined by the link width multiplied by 250MB/s and 500MB/s, as follows:

Slot Size	Bandwidth	Full-Duplex Bandwidth
x1	250MB/s	500MB/s
x4	1GB/s	2GB/s
x8	2GB/s	4GB/s
x16	4GB/s	8GB/s

Scalability is a core feature of PCI Express. PCI Express interface scalability enables greater system operational flexibility and efficiency.

PCI Express devices with different PCI Express link configurations can establish communication using a process called auto-negotiation or link training. If a board with a higher number of lanes is placed in a slot with a lower number of lanes (e.g., a x16 board in a x1 slot) or a board with a lower number of lanes is placed into a slot with a higher number of lanes (e.g., a x4 board into a x16 slot), the link auto-negotiates down to the lower link rate to establish communication. The mechanical option card slots on Trenton PICMG® 1.3 backplanes have PCI Express configuration straps. Some SHB designs may utilize the straps in the PCI Express link width negotiation process.

In order to properly support all of the PCI Express option card slots or devices on a PICMG 1.3 backplane, the SHB must provide an adequate number of both PCI Express links and PCI Express reference clocks.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3.*

SHB AND PICMG® 1.3 BACKPLANE CONFIGURATIONS

The PICMG 1.3 specification enables SHB vendors to provide multiple PCI Express configuration options for edge connectors A and B of a particular SHB. These edge connectors carry the PCI Express links and reference clocks down to the SHB slot on the PICMG 1.3 backplane. The PICMG 1.3 specification states that the SHB must provide as many reference clocks as there are potential PCI Express links on the PICMG 1.3 backplane.

The potential PCI Express link configurations of an SHB fall into two main classifications: server-class and graphics-class. The specific class and PCI Express link configuration of an SHB is determined by the chipset components used on the SHB.

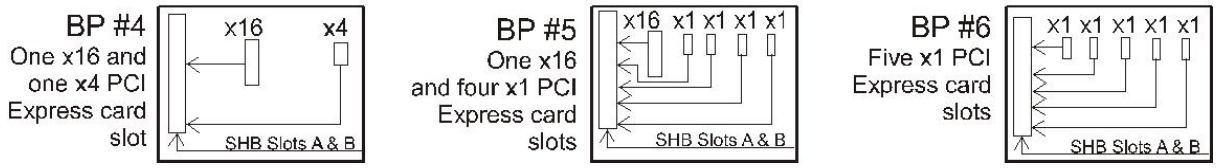
A graphics-class SHB configuration should provide a x16 PCI Express link down to the backplane in order to support high-end PCI Express graphics and video cards. The graphics-class SHB configuration is generally identified by one x16 PCIe link and one x4 or four x1 links to the edge connectors.

NOTE: Graphics-class SHBs should always be used with graphics-class PICMG 1.3 backplanes and server-class SHBs should always be used with server-class PICMG 1.3 backplanes. Combining incompatible SHBs and backplanes will not cause damage to the option cards or SHB, but one or more of the slots may not function and may result in one or more PCI Express option cards on the backplane being non-functional. This is due to the fact that there may not be enough available links to properly connect all of the PCI Express option card slots to the SHB. Precautions have been engineered into the PICMG 1.3 specification to prevent either SHB or backplane damage if this functionality mismatch occurs.

The figures below show some typical SHB and backplane combinations that would result in all of the PCI Express slots successfully establishing communication with the SHB host device.

Graphics-Class SHB:

PCI Express™ Edge Connectors A & B: One x16 and one x4 PCI Express™ Link with five reference clocks



PCI Express link configuration straps for each PCI Express option card slot on a PICMG 1.3 backplane are required as part of the PICMG 1.3 SHB Express™ specification. These configuration straps may be used to alert the SHB as to the specific link configuration expected on each PCI Express option card slot. PCI Express communication between the SHB and option card slots is successful only when there are enough available PCI Express links established between the PICMG 1.3 SHB and each PCI Express slot or device on the backplane.

For more information, refer to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

PCI EXPRESS EDGE CONNECTOR PIN ASSIGNMENTS

Trenton PCI Express server-class backplanes provide edge connectors A, B and C.

Optional I/O signals are defined in the PICMG 1.3 specification and if implemented must be located on edge connector C of the SHB. Trenton PICMG 1.3 backplanes enable some or all of the USB and Ethernet connections on edge connector C, but since these connections are optional, not all SHBs support them. In order to take advantage of these I/O features, the SHB in your system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

The BPG6544 supports two ISA slots via a PCI-to-ISA bridge chip. Since the ISA bus interface is not part of the PICMG 1.3 specification, two reserved pins are used to route the ISA signals SERIRQ and NOGO_ISA to the backplane's PCI-to-ISA bridge chip. Legacy PCI card support is not impacted by this ISA bus signal routing requirement. The following bus pin assignments are used:

* SERIRQ -- connector A, pin B77

** NOGO_ISA -- connector B, pin A2

The following table shows pin assignments for the PCI Express edge connectors on Trenton backplanes. Connector D is only available on graphics-class backplanes.

Connector A			Connector B			Connector C			*Connector D		
	Side B	Side A		Side B	Side A		Side B	Side A		Side B	Side A
1	SMCLK	SMDAT	1	+5Vaux	+5Vaux	1	USB0P	GND	1	INTB#	INTA#
2	GND	GND	2	GND	RSVD **	2	USB0N	GND	2	INTD#	INTC#
3	TDI	TCK	3	a_PETp8	GND	3	GND	USB1P	3	GND	VIO
4	TDO	TMS	4	a_PETn8	GND	4	GND	USB1N	4	REQ3#	GNT3#
5	TRST#	WAKE#	5	GND	a_PERp8	5	USB2P	GND	5	REQ2#	GNT2#
6	PWRBT#	PME#	6	GND	a_PERn8	6	USB2N	GND	6	PCI_RST#	GNT1#
7	PWRGD	PSON#	7	a_PETp9	GND	7	GND	USB3P	7	REQ1#	GNT0#
8	SHB_RST#	PERST#	8	a_PETn9	GND	8	GND	USB3N	8	REQ0#	SERR#
9	CFG0	CFG1	9	GND	a_PERp9	9	USBOC0#	GND	9	SDONE	+3.3V
10	CFG2	CFG3	10	GND	a_PERn9	10	GND	USBOC1#	10	GND	CLKF1
11	RSVD	GND	11	RSVD	GND	11	USBOC2#	GND	11	CLKFO	GND
Mechanical Key			Mechanical Key			Mechanical Key			Mechanical Key		

* Graphics-class backplanes only.

Connector A			Connector B			Connector C			*Connector D		
	Side B	Side A		Side B	Side A		Side B	Side A		Side B	Side A
12	GND	RSVD	12	GND	RSVD	12	GND	USBOC3#	12	CLKC	CLKD
13	b_PETp0	GND	13	a_PETp10	GND	13	NC	GND	13	GND	+3.3V
14	b_PETn0	GND	14	a_PETn10	GND	14	NC	GND	14	CLKA	CLKB
15	GND	b_PERp0	15	GND	a_PER10	15	GND	NC	15	+3.3V	GND
16	GND	b_PERn0	16	GND	a_PERn10	16	GND	NC	16	AD31	GND
17	b_PETp1	GND	17	a_PETp11	GND	17	NC	GND	17	AD29	+3.3V
18	b_PETn1	GND	18	a_PETn11	GND	18	NC	GND	18	M66EN	AD30
19	GND	b_PERp1	19	GND	a_PERp11	19	GND	NC	19	AD27	AD28
20	GND	b_PERn1	20	GND	a_PERn11	20	GND	NC	20	AD25	GND
21	b_PETp2	GND	21	a_PETp12	GND	21	a_MDI0p	GND	21	GND	AD26
22	b_PETn2	GND	22	a_PETn12	GND	22	a_MDI0n	GND	22	C/BE3#	AD24
23	GND	b_PERp2	23	GND	a_PERp12	23	GND	a_MDI1p	23	AD23	+3.3V
24	GND	b_PERn2	24	GND	a_PERn12	24	GND	a_MDI1n	24	GND	AD22
25	b_PETp3	GND	25	a_PETp13	GND	25	a_MDI2p	GND	25	AD21	AD20
26	b_PETn3	GND	26	a_PETn13	GND	26	a_MDI2n	GND	26	AD19	PCIXCAP
27	GND	b_PERp3	27	GND	a_PERp13	27	GND	a_MDI3p	27	+5V	AD18
28	GND	b_PERn3	28	GND	a_PERn13	28	GND	a_MDI3n	28	AD17	AD16
29	REFCLK0+	GND	29	a_PETp14	GND	29	IPMB_CL	GND	29	C/BE2#	GND
30	REFCLK0-	GND	30	a_PETn14	GND	30	IPMB_DA	GND	30	PCI_PRST#	FRAME#
31	GND	REFCLK1+	31	GND	a_PERp14	31	NC	NC	31	IRDY#	TRDY#
32	RSVD-G	REFCLK1-	32	GND	a_PERn14	32	NC	NC	32	DEVSEL#	+5V
33	REFCLK2+	GND	33	a_PETp15	GND	33	NC	NC	33	LOCK#	STOP#
34	REFCLK2-	GND	34	a_PETn15	GND	34	b_MDI0p	GND	34	PERR#	GND
35	GND	REFCLK3+	35	GND	a_PERp15	35	b_MDI0n	GND	35	GND	C/BE1#
36	RSVD-G	REFCLK3-	36	GND	a_PERn15	36	GND	b_MDI1p	36	PAR	AD14
37	REFCLK4+	GND	37	RSVD	GND	37	GND	b_MDI1n	37	SB0#	GND
38	REFCLK4-	GND	38	RSVD	RSVD	38	b_MDI2	GND	38	GND	AD12
39	GND	REFCLK5+	39	GND	GND	39	b_MDI2n	GND	39	AD15	AD10
40	RSVD-G	REFCLK5-	40	GND	GND	40	GND	b_MDI3p	40	AD13	GND
41	REFCLK6+	GND	41	GND	GND	41	GND	b_MDI3n	41	GND	AD09
42	REFCLK6-	GND	42	GND	GND	42	+3.3V	+3.3V	42	AD11	C/BE0#
43	GND	REFCLK7+	43	GND	GND	43	+3.3V	+3.3V	43	AD08	GND
44	GND	REFCLK7-	44	+12V	+12V	44	+3.3V	+3.3V	44	GND	AD06
45	a_PETp0	GND	45	+12V	+12V	45	+3.3V	+3.3V	45	AD07	AD05
46	a_PETn0	GND	46	+12V	+12V	46	+3.3V	+3.3V	46	AD04	GND
47	GND	a_PERp0	47	+12V	+12V	47	+3.3V	+3.3V	47	GND	AD02
48	GND	a_PERn0	48	+12V	+12V	48	+3.3V	+3.3V	48	AD03	AD01
49	a_PETp1	GND	49	+12V	+12V	49	+3.3V	+3.3V	49	AD00	GND
50	a_PETn1	GND				50	+3.3V	+3.3V			
51	GND	a_PERp1				51	GND	GND			
52	GND	a_PERn1				52	GND	GND			
53	a_PETp2	GND				53	GND	GND			
54	a_PETn2	GND				54	GND	GND			
55	GND	a_PERp2				55	GND	GND			
56	GND	a_PERn2				56	GND	GND			
57	a_PETp3	GND				57	GND	GND			
58	a_PETn3	GND				58	GND	GND			
59	GND	a_PERp3				59	+5V	+5V			
60	GND	a_PERn3				60	+5V	+5V			
61	a_PETp4	GND				61	+5V	+5V			
62	a_PETn4	GND				62	+5V	+5V			
63	GND	a_PERp4				63	GND	GND			
64	GND	a_PERn4				64	GND	GND			
65	a_PETp5	GND				65	GND	GND			
66	a_PETn5	GND				66	GND	GND			
67	GND	a_PERp5				67	GND	GND			
68	GND	a_PERn5				68	GND	GND			
69	a_PETp6	GND				69	GND	GND			
70	a_PETn6	GND				70	GND	GND			
71	GND	a_PERp6				71	GND	GND			
72	GND	a_PERn6				72	GND	GND			
73	a_PETp7	GND				73	+12V	+12V			
74	a_PETn7	GND				74	+12V	+12V			
75	GND	a_PERp7				75	+12V	+12V			
76	GND	a_PERn7				76	+12V	+12V			
77	RSVD *	GND				77	+12V	+12V			
78	+3.3V	+3.3V				78	+12V	+12V			
79	+3.3V	+3.3V				79	+12V	+12V			
80	+3.3V	+3.3V				80	+12V	+12V			
81	+3.3V	+3.3V				81	+12V	+12V			
82	+3.3V	+3.3V				82	+12V	+12V			

* Graphics-class backplanes only.

PCI EXPRESS SIGNALS OVERVIEW

The following table provides a description of the SHB slot signal groups on the PCI Express connectors.

Type	Signals	Description	Connector	Source
Global	GND, +5V, +3.3V, +12V	Power		Backplane
	PSON#	Optional ATX support	A	SHB
	PWRGD, PWRBT#, +5Vaux	Optional ATX support	A and B	Backplane
	TRST#, TCK, TMS, TDI	Optional JTAG support	A	Backplane
	TDO	Optional JTAG support	A	SHB
	SMCLK, SMDAT	Optional SMBus support	A	SHB & Backplane
	VIO	Match keying for PCI bus	D	Backplane
	IPMB_CL, IPMB_DA	Optional IPMB support	C	Backplane
	CFG[0:3]	PCIe configuration straps	A	SHB & Backplane
	SHB_RST#	Optional reset line	A	Backplane
	RSVD	Reserved	A and B	Backplane
	RSVD-G	Reserved ground	A	SHB
	WAKE#	Signal for link reactivation	A	Backplane
PCIe	a_PETp[0:15] a_PETn[0:15] a_PERp[0:15] a_PERn[0:15]	Point-to-point from SHB slot through the x16 PCIe connector (A) to the target device(s)	A and B	SHB & Backplane
	b_PETp[0:3] b_PETn[0:3] b_PERp[0:3] b_PERn[0:3]	Point-to-point from SHB slot through the x8 PCIe connector (B) to the target device(s)	A	SHB & Backplane
	REFCLK[0:7]+ REFCLK[0:7]-	Clock synchronization of PCIe expansion slots	A	
	PERST#	PCIe fundamental reset	A	SHB & Backplane
PCI(-X)	AD[0:31], FRAME#, IRDY#, TRDY#, STOP#, LOCK#, DEVSEL#, PERR#, SERR#, C/BE[0:3], SDONE, SBO#, PAR	Bussed on SHB slot and expansion slots	D	SHB & Backplane
	GNT[0:3], REQ[0:3], CLKA, CLKB, CLKC, CLKD, CLKFO, CLKFI	Point-to-point from SHB slot to each expansion slot	D	SHB & Backplane
	INTA#, INTB#, INTC#, INTD#	Bussed (rotating) on SHB slot and expansion slots	D	Backplane
	M66EN, PCIXCAP	Bussed on SHB slot and expansion slots	D	Backplane
	PCI_PRST#	PCI(-X) present on backplane detect	D	Backplane
	PME#	Optional PCI wake-up event bussed on SHB and backplane expansion slots	A	Backplane

PCI EXPRESS SIGNALS OVERVIEW (CONTINUED)

Type	Signals	Description	Connector	Source
Misc. I/O *	USB[0:3]P, USB[0:3]N, USBOC[0:3]#	Optional point-to-point from SHB Connector C to a destination USB device	C	SHB & Backplane
	a_MDI[0:3]p a_MDI[0:3]n b_MDI[0:3]p b_MDI[0:3]n	Optional point-to-point from SHB Connector C to a destination Ethernet device	C	SHB & Backplane

* According to the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*, some of these I/O connections are optional, and therefore not all SHBs support them. Check with the SHB vendor for a listing of I/O connections which are supported by the SHB.

POWER CONNECTION

The combination of new power supply technologies and the system capabilities defined in the SHB Express™ (PICMG® 1.3) specification require a different approach to connecting system power to a PICMG 1.3 backplane and/or SHB hardware.

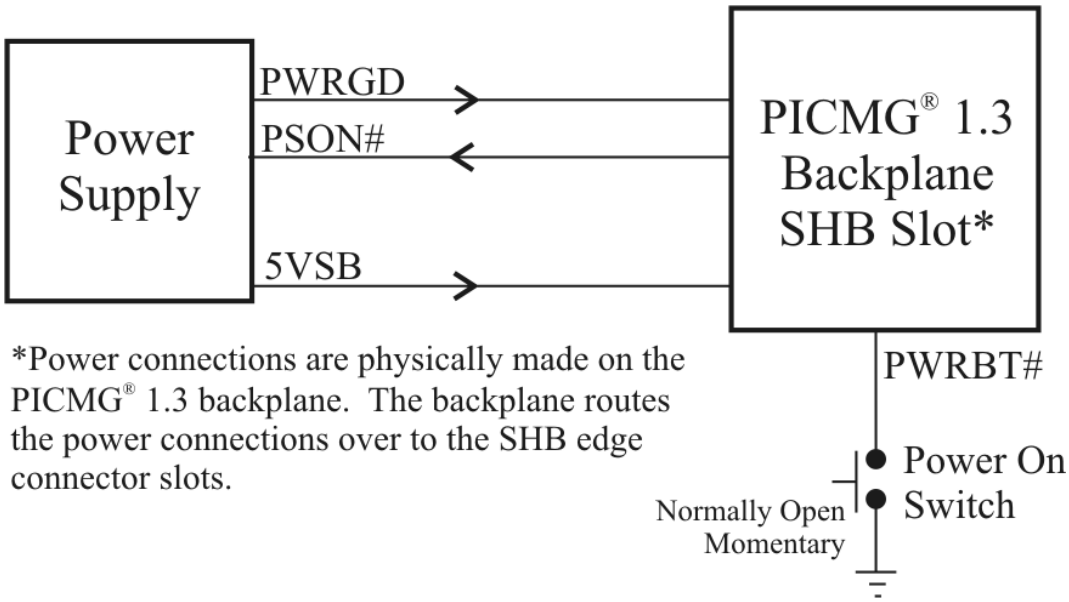
To improve system MTTR (Mean Time To Repair), the PICMG 1.3 specification defines power connections to the SHB's edge connectors which should provide enough power to the SHB to eliminate the need to connect auxiliary power to the SHB. The connectors on a backplane must have an adequate number of contacts that are sufficiently rated to safely deliver the necessary power to drive high-performance SHBs. Trenton PICMG 1.3 backplanes define ATX/EPS and +12V connectors that are compatible with today's ATX/EPS power supply cable harnesses and provide multiple pins capable of delivering the current necessary to power high-performance processors.

The PICMG 1.3 specification supports soft power control signals via the Advanced Configuration and Power Interface (ACPI). Trenton SHBs support these signals, which are controlled by the ACPI and are used to implement various sleep modes. Refer to the General ACPI Configuration section of the *Advanced Setup* chapter in your SHB manual for information on ACPI BIOS settings.

When soft control signals are implemented, the type of ATX or EPS power supply used in the system and the operating system software will dictate how system power should be connected to the SHB. It is critical that the correct method be used.

POWER SUPPLY AND SHB INTERACTION

The following diagram illustrates the interaction between the power supply and the processor. The signals shown are PWRGD (Power Good), PSON# (Power Supply On), 5VSB (5 Volt Standby) and PWRBT# (Power Button). The +/- 12V, +/-5V, +3.3V and Ground signals are not shown.



Power Supply and SHB Interaction

PWRGD, PSON# and 5VSB are usually connected directly from an ATX or EPS power supply to the backplane. The PWRBT# is a normally open momentary switch that can be wired directly to a power button on the chassis.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

ELECTRICAL CONNECTION CONFIGURATIONS

There are a number of different connector types, such as EPS, ATX or terminal blocks, which can be utilized in wiring power supply and control functions to a PICMG 1.3 backplane. However, there are only two basic electrical connection configurations.

ACPI Connection

The diagram above shows how to connect an ACPI compliant power supply to an ACPI enabled PICMG 1.3 system. The following table shows the required connections which must be made for soft power control to work.

Signal	Description	Source
+ 12V	DC voltage for those systems that require it	Power Supply
+ 5V	DC voltage for those systems that require it	Power Supply
+ 3.3V	DC voltage for those systems that require it	Power Supply
+ 5VSB	5 Volt Standby. This DC voltage is always on when an ATX or EPS type power supply has AC voltage connected. 5VSB is used to keep the necessary circuitry functioning for software power control and wake up.	Power Supply
PWRGD	Power Good. This signal indicates that the power supply's voltages are stable and within tolerance.	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply.	SHB/Backplane
PWRBT#	Power Button. A momentary normally open switch is connected to this signal. When pressed and released, this signals the SHB to turn on a power supply that is in an off state. If the system is on, holding this button for four seconds will cause the SHB's chipset to shut down the power supply. The operating system is not involved and therefore this is not considered a clean shutdown. Data can be lost if this situation occurs.	Power Button

Legacy Non-ACPI Connection

For system integrators that either do not have or do not require an ACPI compliant power supply as described in the section above, an alternative electrical configuration is described in the following table.

Signal	Description	Source
+ 12V	DC voltage for those systems that require it	Power Supply
+ 5V	DC voltage for those systems that require it	Power Supply
+ 3.3V	DC voltage for those systems that require it	Power Supply
+ 5VSB	Not required	Power Supply
PWRGD	Not required	Power Supply
PSON#	Power Supply On. This signal is used to turn on an ATX or EPS type power supply. If an ATX or EPS power supply is used in this legacy configuration, a shunt must be installed on the backplane from PSON# to signal Ground. This forces the power supply DC outputs on whenever AC to the power supply is active.	Backplane
PWRBT#	Not used	

In addition to these connections, there is usually a switch controlling AC power input to the power supply.

This page intentionally left blank.

Chapter 4 - Graphics-Class Backplanes

6532-000 BPG2/2

The BPG2/2 is a PICMG® 1.3 compliant, small form factor, graphics-class backplane made up of a six-layer .062" thick PCB.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has a x16 PCI Express slot (PCIe2) which provides the mechanical connection between the PCI Express option card and the SHB. This slot is driven by the SHB via a x16 PCI Express link (A0) and mechanically can support x16, x8, x4 and x1 PCI Express cards.

In addition, the BPG2/2 has two PCI-X slots (SLTA1 and SLTB1) which are connected to the SHB by a x4 PCI Express link (B0) via a PCI Express-to-PCI-X bridge chip which provides two 64-bit/133MHz PCI-X channels. The PCI-X slots provide support for PCI-X option cards and PCI option cards, which must be either +3.3V or universal option cards. If a card with an interface bus speed less than 133MHz is placed in either of the PCI-X slots, the bridge chip throttles down the bus interface speed to match that of the card.

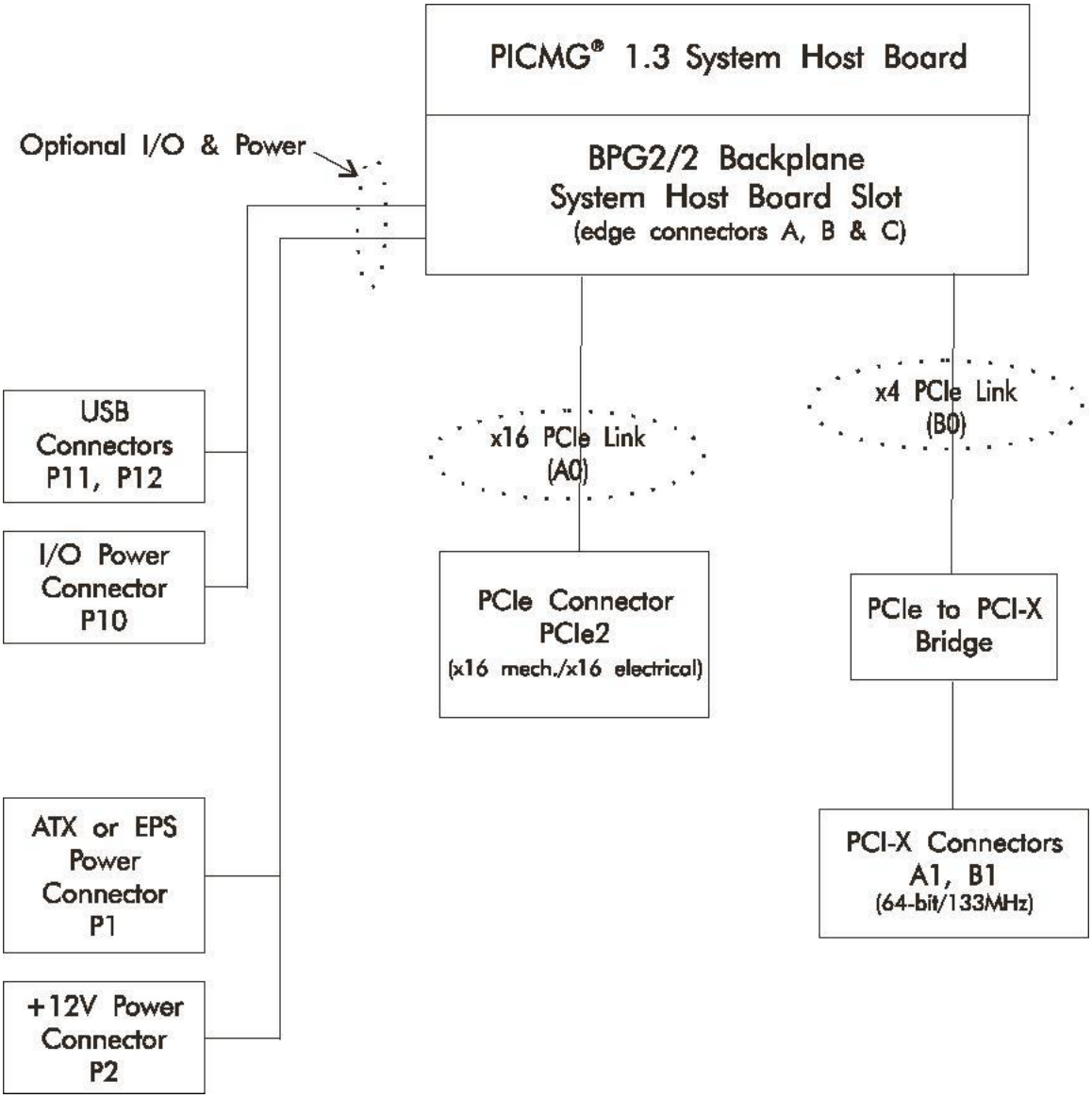
The BPG2/2 has two USB 2.0 headers which are capable of supporting up to four USB 2.0 ports on the backplane. USB functionality on the BPG2/2 is dependent on the SHB providing I/O capability to edge connector C of the backplane. In order to take advantage of the USB capability, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

The backplane has a power connector (P1) which can accommodate either ATX or EPS power. A +12V power connector (P2) is provided for routing auxiliary power to the SHB's edge connectors, eliminating the need for auxiliary power connections on the system host board.

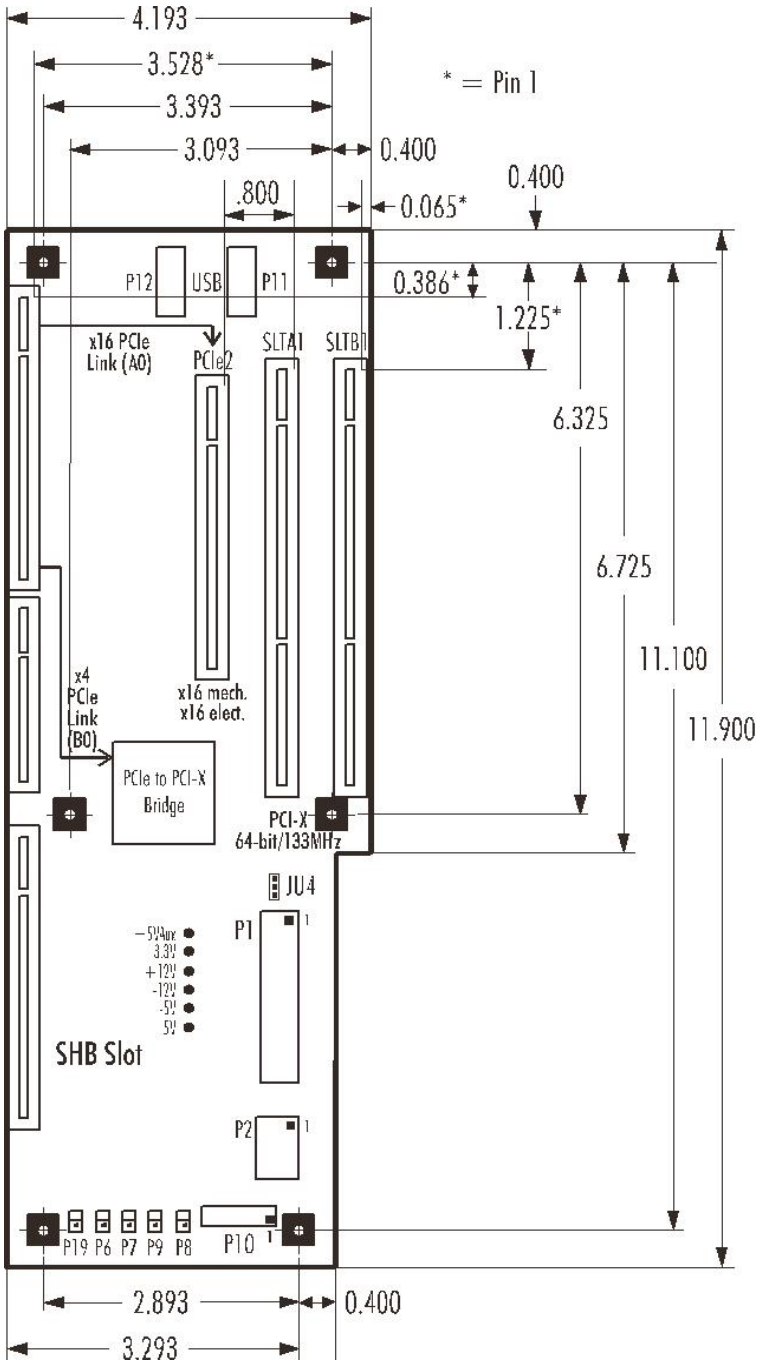
The BPG2/2 backplane is available in models which have either right angle or straight-in power connections.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

6532-000 BPG2/2 BLOCK DIAGRAM



6532-000 BPG2/2 DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "TOP" and "BOTTOM" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the TOP if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the BOTTOM if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

BPG2/2 CONNECTORS

The connectors available on the BPG2/2 vary depending on the version of the backplane you have. Connectors for the 6532-007 (right angle connectors) and 6532-008 (straight- in connectors) are defined below.

6532-007 BPG2/2-CRA CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin right angle dual row header, Amp #794516-1

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

6532-007 BPG2/2-CRA CONNECTORS (CONTINUED)

P2 - +12V Power Connector

8 pin right angle mini fit JR, Molex #39-30-0080

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P6 - Power-On Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#

6532-007 BPG2/2-CRA CONNECTORS (CONTINUED)

P10 - I/O Power Connector (continued)

Pin	Signal	Pin	Signal
15	PWRGD	16	+5VAUX
17	Gnd	18	+5VAUX
19	Gnd	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P19 - System Management Bus Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SMB Clock
2	SMB Data

6532-008 BPG2/2-CST CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin dual row mini fit JR, Molex #39-29-6248

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd

6532-008 BPG2/2-CST CONNECTORS (CONTINUED)

P1 - ATX/EPS Power Connector (continued)

Pin	Signal	Pin	Signal
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P2 - +12V Power Connector

8 pin mini fit JR, Molex #39-29-3086

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P6 - Power-On Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRGD
2	Gnd

6532-008 BPG2/2-CST CONNECTORS (CONTINUED)

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	+5VAUX
17	Gnd	18	+5VAUX
19	Gnd	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P19 - System Management Bus Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SMB Clock
2	SMB Data

6537-000 BPG4

The BPG4 is a PICMG® 1.3 compliant, small form factor, graphics-class backplane made up of a six-layer .062" thick PCB.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has a PCI Express expansion slot (PCIeS) which is a x8 slot that mechanically connects a Trenton IOB31 I/O expansion board to the backplane, providing an additional x1 PCI Express link from a graphics-class SHB.

The three remaining PCIe slots provide the mechanical connections between the PCI Express option cards and either the SHB or the PCIeS slot. The first slot (PCIe1), which connects to the PCIeS slot, is a x8 slot which mechanically can support x8, x4 and x1 PCI Express cards. Slot PCIe1 provides a x1 PCI Express electrical interface. The second slot (PCIe2) connects to the SHB and provides a x4 PCIe link (B0) between the SHB and the backplane. It is a x8 slot which mechanically can support x8, x4 and x1 PCI Express cards.

NOTE: In order to use slot PCIe1 when you are using a Trenton PCI Express SHB, you must have a Trenton IOB31 (6474-000) I/O expansion board on the SHB. The IOB31 enables communication between the SHB and slot PCIe1 by providing a x1 or x4 PCI Express link to the PCIeS slot, depending on the capabilities of the SHB.

PCI Express slot PCIe3 is driven by a x16 PCI Express link (A0) from the SHB and mechanically can support x16, x8, x4 and x1 PCI Express cards.

The BPG4 supports the optional Ethernet routing feature of the SHB Express specification and provides two 10/100/1000Base-T Ethernet RJ-45 connectors. It also has two USB 2.0 headers which are capable of supporting up to four USB 2.0 ports on the backplane.

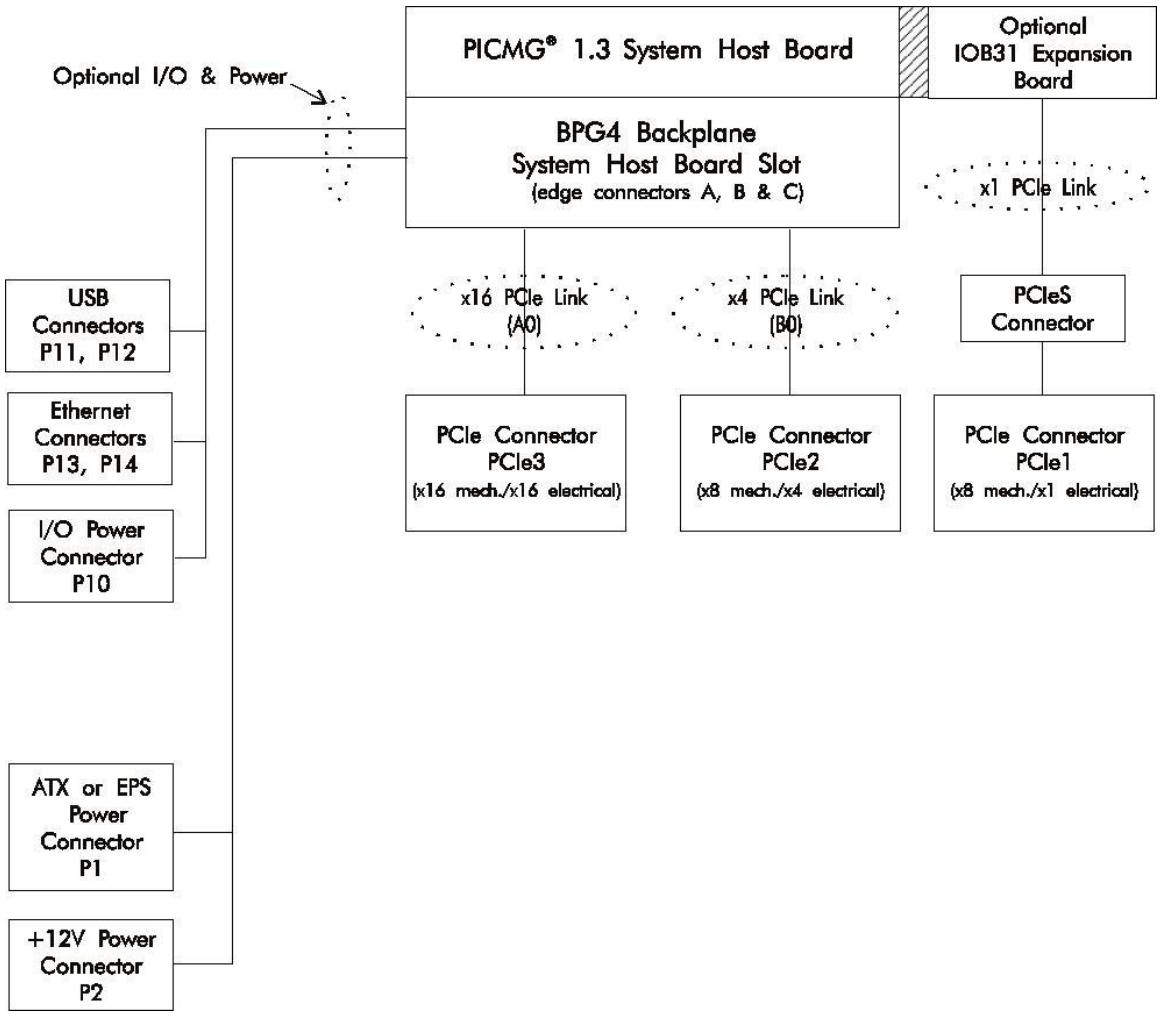
USB and Ethernet functionality on the BPG4 is dependent on the SHB providing I/O capability to edge connector C of the backplane. In order to take advantage of these I/O features, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

The backplane has a power connector (P1) which can accommodate either ATX or EPS power. A +12V power connector (P2) is provided for routing auxiliary power to the SHB's edge connectors, eliminating the need for auxiliary power connections on the system host board.

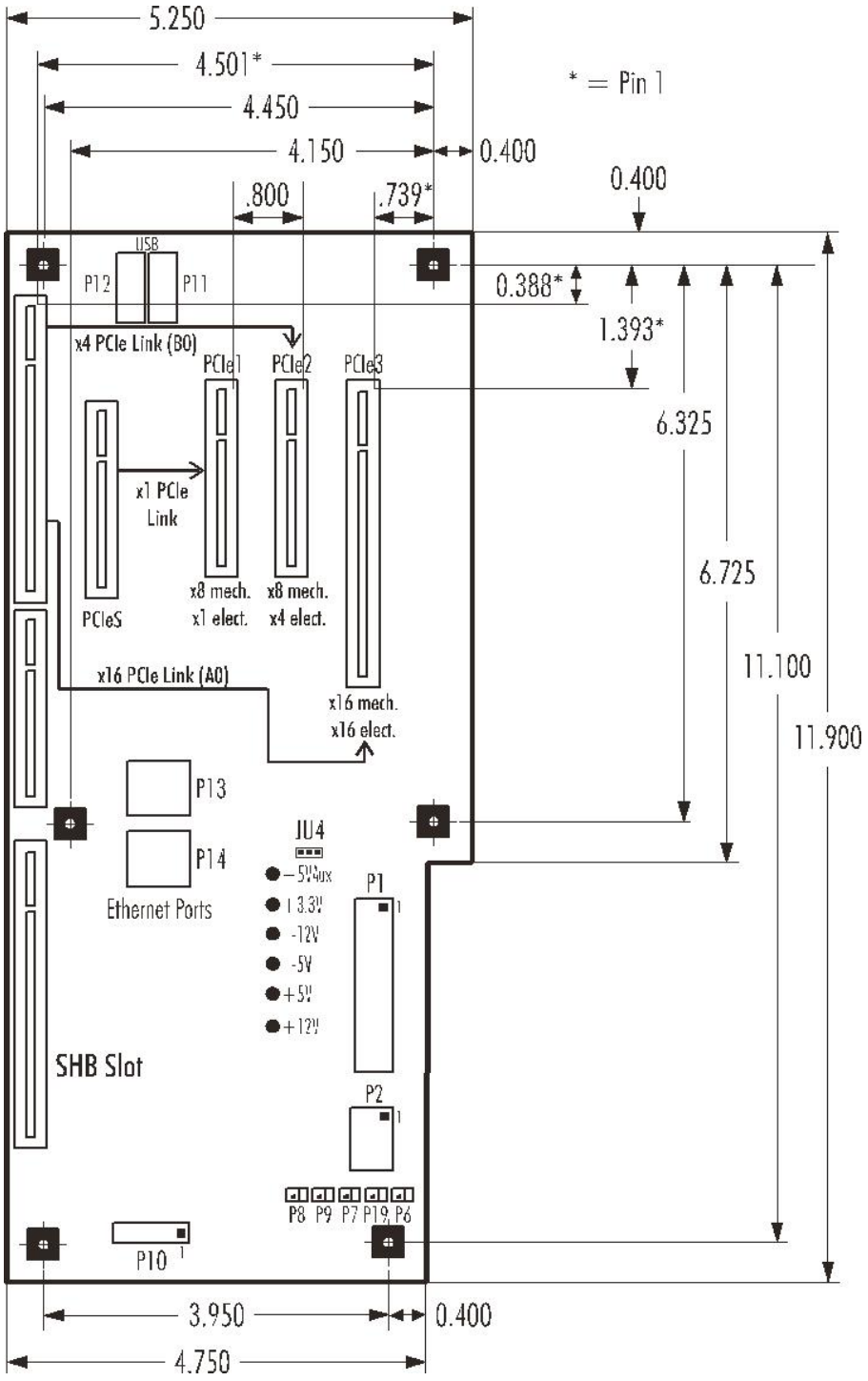
The BPG4 backplane is available in models which have either right angle or straight-in power connections.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

6537-000 BPG4 BLOCK DIAGRAM



6537-000 BPG4 DIMENSIONAL DRAWING



PCB thickness .062”
Mounting holes .156” diameter
Connector spacing .800” centers

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

BPG4 CONNECTORS

The connectors available on the BPG4 vary depending on the version of the backplane you have. Connectors for the 6537-007 (right angle connectors) and 6537-008 (straight- in connectors) are defined below.

6537-007 BPG4-CRA CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin right angle dual row header, Amp #794516-1

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

6537-007 BPG4-CRA CONNECTORS (CONTINUED)

P2 - +12V Power Connector

8 pin right angle mini fit JR, Molex #39-30-0080

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#

6537-007 BPG4-CRA CONNECTORS (CONTINUED)

P10 - I/O Power Connector (continued)

Pin	Signal	Pin	Signal
15	PWRGD	16	+5VAUX
17	Gnd	18	+5VAUX
19	Gnd	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RA RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RA RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+

6537-007 BPG4-CRA CONNECTORS (CONTINUED)

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1 (cont'd)

Pin	Signal
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - System Management Bus Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

6537-008 BPG4-CST CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin dual row mini fit JR, Molex #39-29-6248

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P2 - +12V Power Connector

8 pin mini fit JR, Molex #39-29-3086

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

6537-008 BPG4-CST CONNECTORS (CONTINUED)

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	+5VAUX
17	Gnd	18	+5VAUX
19	Gnd	20	-12V

6537-008 BPG4-CST CONNECTORS (CONTINUED)

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RA RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RA RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

6537-008 BPG4-CST CONNECTORS (CONTINUED)

P19 - System Management Bus Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

6544-000 BPG6544

The BPG6544 is a PICMG® 1.3 compliant, 14-slot form factor, graphics-class backplane made up of a six-layer .080" thick PCB. The backplane supports Trenton and PICMG® 1.3 14-slot (64-bit) hole patterns.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has a PCI Express expansion slot (PCIeS) which is a x8 slot that mechanically connects a Trenton IOB31 I/O expansion board to the backplane, providing an additional x1 PCI Express link from a graphics-class SHB.

The two remaining PCIe slots provide the mechanical connections between the PCI Express option cards and either the SHB or the PCIeS slot. The first slot (PCIe1) is a x8 slot which mechanically can support x8, x4 and x1 PCI Express cards and is driven by a x1 electrical interface from the PCIeS slot. The second slot (PCIe2) connects to the SHB and provides a x16 PCIe link (A0) between the SHB and the backplane. It is a x16 slot which mechanically can support x16, x8, x4 and x1 PCI Express cards.

NOTE: In order to use slot PCIe1 when you are using a Trenton PCI Express SHB, you must have a Trenton IOB31 (6474-000) I/O expansion board on the SHB. The IOB31 enables communication between the SHB and slot PCIe1 by providing a x1 PCI Express link to the PCIeS slot.

The BPG6544 has five PCI-X slots which are connected to the SHB by a x4 PCI Express link (B0) via a PCI Express-to-PCI-X bridge chip, which supports four 64-bit/66MHz PCI-X slots and one 64-bit/133MHz PCI-X slot. The PCI-X slots provide support for PCI-X option cards and PCI option cards, which must be either +3.3V or universal option cards. If a card has an interface bus speed lower than the speed of the PCI-X slot in which it is placed, the bridge chip throttles down the bus interface speed to match that of the card.

NOTE: The 64-bit/66MHz PCI-X slots enable 66MHz PCI-X option cards to run at 66MHz. 66MHz PCI option cards will function in these slots but may only operate at 33MHz due to the differences between a PCI and PCI-X bus.

In addition, the BPG6544 supports optional SHB edge connector D, which provides a 32-bit/33MHz PCI interface to drive two PCI slots. This PCI interface also connects to a PCI-to-ISA bridge chip to support two ISA slots, which support legacy ISA and 32-bit/ 33MHz PCI option cards. Since the ISA bus interface is not part of the PICMG 1.3 specification, two reserved pins are used to route the ISA signals SERIRQ (connector A, pin B77) and NOGO_ISA (connector B, pin A2) to the backplane's PCI-to-ISA bridge chip. As a result, if a third-party SHB does not support this required ISA signal routing, the BPG6544 backplane's ISA card slots will not function. Legacy PCI card support is not impacted by this ISA bus signal routing requirement.

The BPG6544 supports the optional Ethernet routing feature of the SHB Express specification and provides two 10/100/1000Base-T Ethernet RJ-45 connectors. It also has two USB 2.0 headers which are capable of supporting up to four USB 2.0 ports on the backplane.

USB and Ethernet functionality on the BPG6544 is dependent on the SHB providing I/O capability to edge connector C of the backplane. In order to take advantage of these I/O features, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

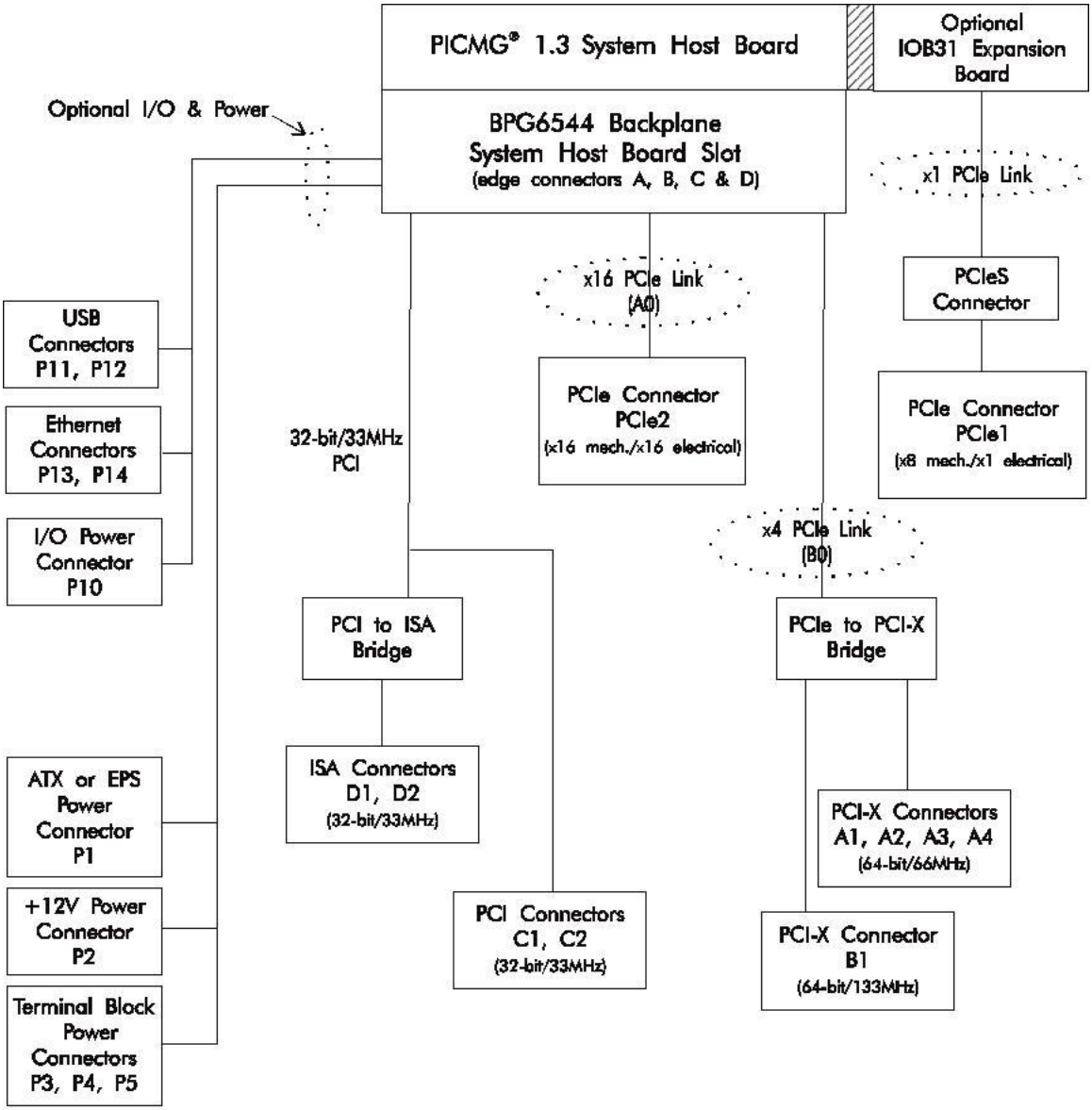
The backplane has a power connector (P1) which can accommodate either ATX or EPS power. A +12V power connector (P2) is provided for routing auxiliary power to the SHB's edge connectors, eliminating the need for auxiliary power connections on the system host board. The BPG6544 also has three extended-

current terminal block connectors which provide additional power capacity for power-intensive applications -- up to 80 Amps of +12V, 120 Amps of +3.3V and 80 Amps of +5V.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; “green” indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

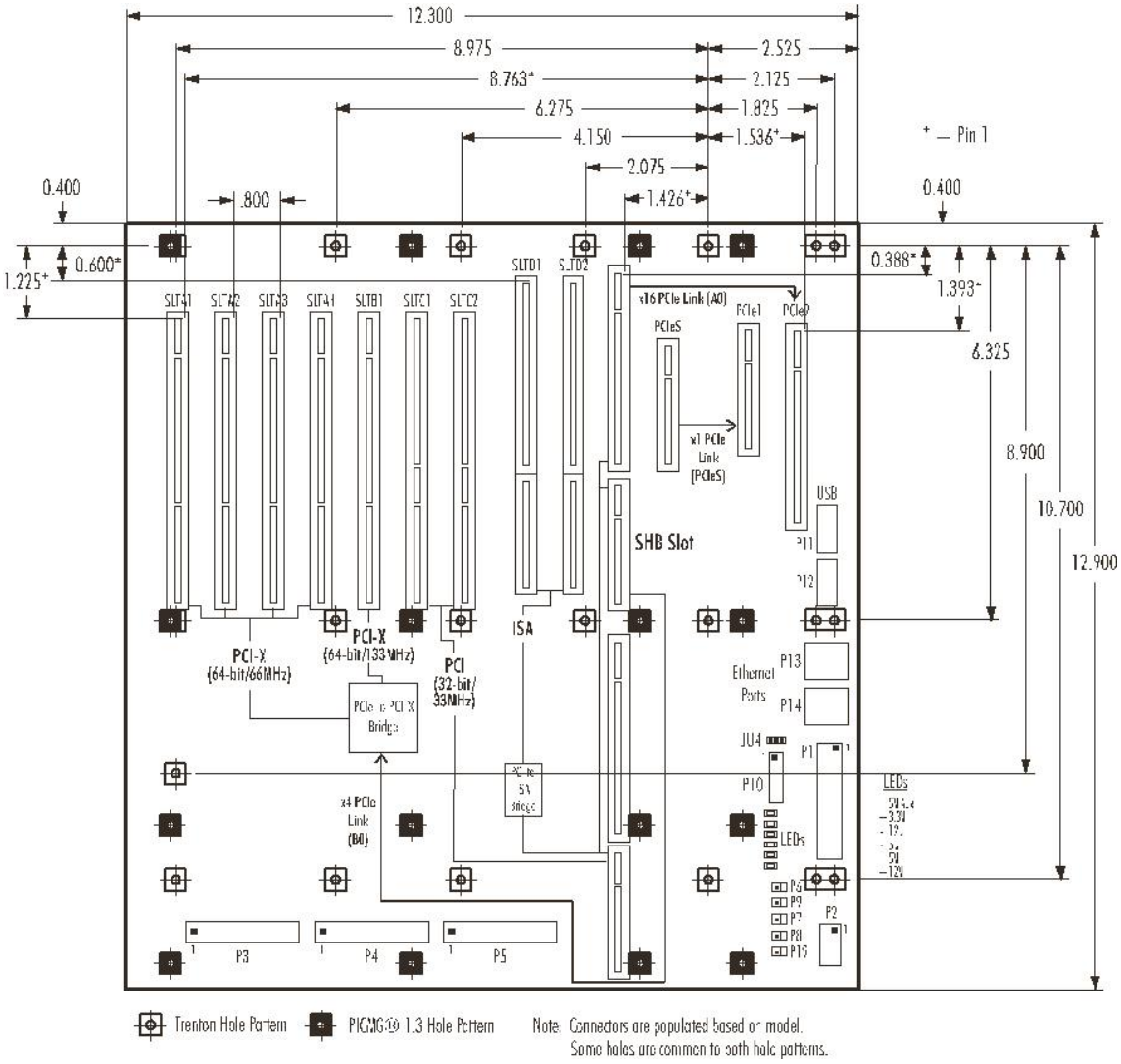
Models with other power configurations may be available. Contact Trenton Technology for more information.

6544-000 BPG6544 BLOCK DIAGRAM



6544-000 BPG6544 DIMENSIONAL DRAWINGS

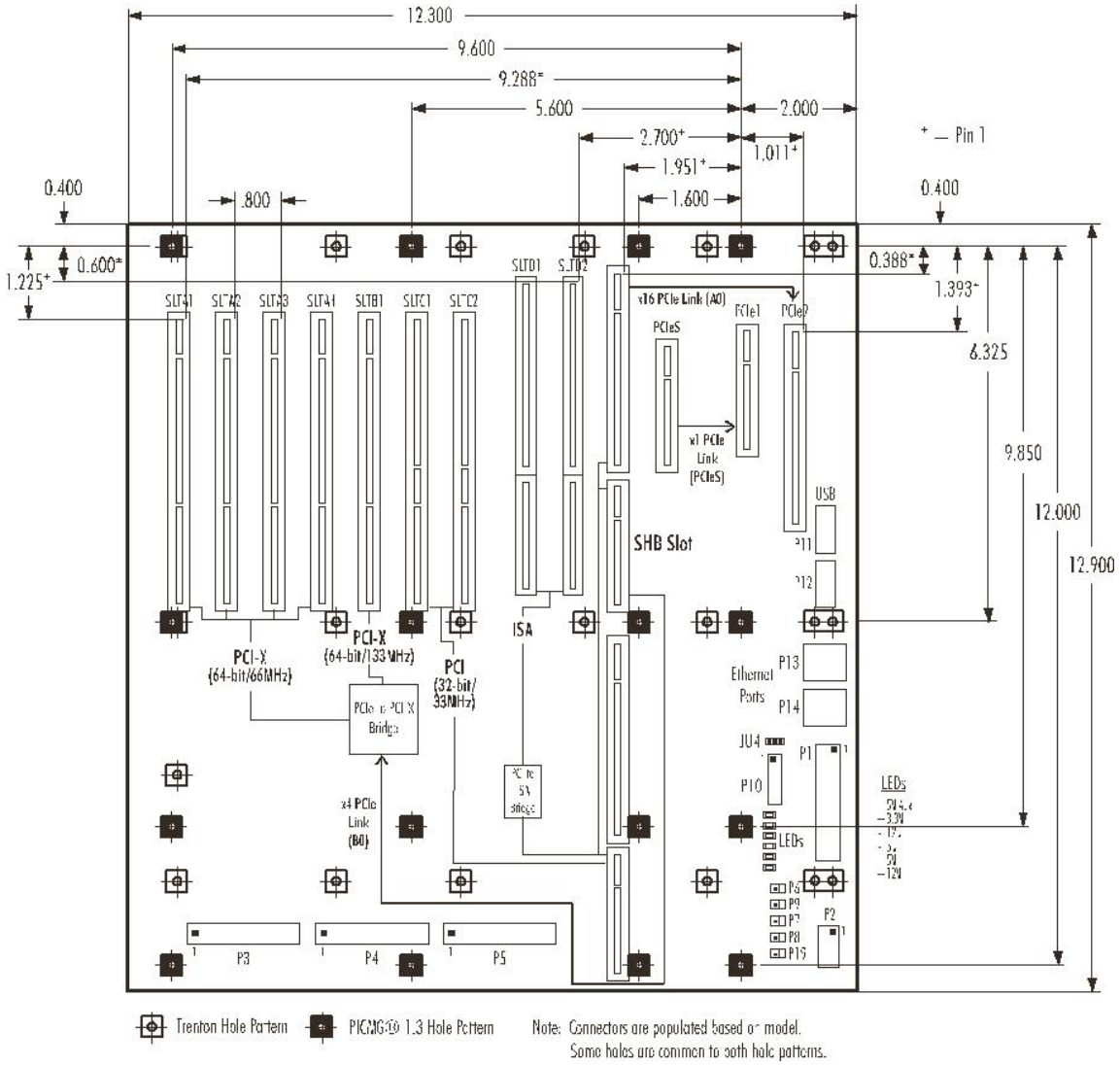
Trenton 14-Slot Hole Pattern



PCB thickness .080”
Mounting holes .156” diameter
Connector spacing .800” centers

6544-000 BPG6544 DIMENSIONAL DRAWINGS

PICMG® 1.3 14-Slot Hole Pattern



PCB thickness .080”
Mounting holes .156” diameter
Connector spacing .800” centers

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

BPG6544 CONNECTORS

The connectors available on the BPG6544 vary depending on the version of the backplane you have. Connectors for the 6544-003 (-E+A) and 6544-004 (-EPS) are defined below.

6544-003 BPG6544-E+A CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - EPS Power Connector

24 pin dual row header, Molex #44206-0007

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

6544-003 BPG6544-E+A CONNECTORS (CONTINUED)

P2 - +12V Power Connector

4 pin mini fit JR, Molex #39-29-3046

Pin	Signal	Pin	Signal
1	Gnd	3	+12V
2	Gnd	4	+12V

P3 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	Gnd
6	Gnd
7	+12V
8	+12V
9	+12V
10	+12V

P4 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	Gnd
2	+3.3V
3	+3.3V
4	+3.3V
5	+3.3V
6	+3.3V
7	+3.3V
8	+3.3V
9	Gnd
10	Gnd

P5 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd
6	Gnd

6544-003 BPG6544-E+A CONNECTORS (CONTINUED)

P5 - Terminal Block Connector (continued)

Pin	Signal
7	Gnd
8	Gnd
9	Gnd
10	Gnd

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin dual row header, Molex #87831-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#

6544-003 BPG6544-E+A CONNECTORS (CONTINUED)

P10 - I/O Power Connector (continued)

Pin	Signal	Pin	Signal
15	PWRGD	16	+5VAUX_IN
17	Gnd	18	+5VAUX_IN
19	Gnd	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RA RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

6544-003 BPG6544-E+A CONNECTORS (CONTINUED)

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RA RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - System Management Bus Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

6544-004 BPG6544-EPS CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - EPS Power Connector

24 pin dual row header, Molex #44206-0007

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P2 - +12V Power Connector

8 pin mini fit JR, Molex #39-29-3086

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

6544-004 BPG6544-EPS CONNECTORS (CONTINUED)

P3 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	+5V
4	+5V
5	Gnd
6	Gnd
7	+12V
8	+12V
9	+12V
10	+12V

P4 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	Gnd
2	+3.3V
3	+3.3V
4	+3.3V
5	+3.3V
6	+3.3V
7	+3.3V
8	+3.3V
9	Gnd
10	Gnd

P5 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	Gnd
2	Gnd
3	Gnd
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	Gnd

6544-004 BPG6544-EPS CONNECTORS (CONTINUED)

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin dual row header, Molex #87831-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	+5VAUX_IN
17	Gnd	18	+5VAUX_IN
19	Gnd	20	-12V

6544-004 BPG6544-EPS CONNECTORS (CONTINUED)

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RJ-45 connector, Molex #85508-0001

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RJ-45 connector, Molex #85508-0001

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

6544-004 BPG6544-EPS CONNECTORS (CONTINUED)

P19 - System Management Bus Connector
2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

6600-000 BPG6600

The BPG6600 is a PICMG® 1.3 compliant, 14-slot form factor, graphics-class backplane made up of a six-layer .080" thick PCB. The backplane supports Trenton and PICMG® 1.3 14-slot hole patterns.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has a PCI Express expansion slot (PCIeS) which is a x8 slot that mechanically connects a Trenton IOB31 I/O expansion board to the backplane, providing an additional x1 PCI Express link from a graphics-class SHB.

The two remaining PCIe slots provide the mechanical connections between the PCI Express option cards and either the SHB or the PCIeS slot. The first slot (PCIe1) is a x8 slot which mechanically can support x8, x4 and x1 PCI Express cards and is driven by a x1 electrical interface from the PCIeS slot. The second slot (PCIe2) connects to the SHB and provides a x16 PCIe link (A0) between the SHB and the backplane. It is a x16 slot which mechanically can support x16, x8, x4 and x1 PCI Express cards.

NOTE: In order to use slot PCIe1 when you are using a Trenton PCI Express SHB, you must have a Trenton IOB31 (6474-000) I/O expansion board on the SHB. The IOB31 enables communication between the SHB and slot PCIe1 by providing a x1 PCI Express link to the PCIeS slot.

The BPG6600 has six PCI-X slots which are connected to the SHB by a x4 PCI Express link (B0) which drives a PCI Express-to-PCI-X bridge chip, which supports four 64-bit/ 66MHz PCI-X slots and two 64-bit/100MHz PCI-X slots. The PCI-X slots provide support for PCI-X option cards and PCI option cards, which must be either +3.3V or universal option cards. If a card has an interface bus speed lower than the speed of the PCI-X slot in which it is placed, the bridge chip throttles down the bus interface speed to match that of the card.

NOTE: The 64-bit/66MHz PCI-X slots enable 66MHz PCI-X option cards to run at 66MHz. 66MHz PCI option cards will function in these slots but may only operate at 33MHz due to the differences between a PCI and PCI-X bus.

In addition, the BPG6600 supports optional SHB edge connector D, which provides a 32-bit/33MHz PCI interface to drive four PCI slots, which can accommodate +5V only or universal 32-bit/33MHz PCI option cards.

The BPG6600 supports the optional Ethernet routing feature of the SHB Express specification and provides two 10/100/1000Base-T Ethernet RJ-45 connectors. It also has two USB 2.0 headers which are capable of supporting up to four USB 2.0 ports on the backplane.

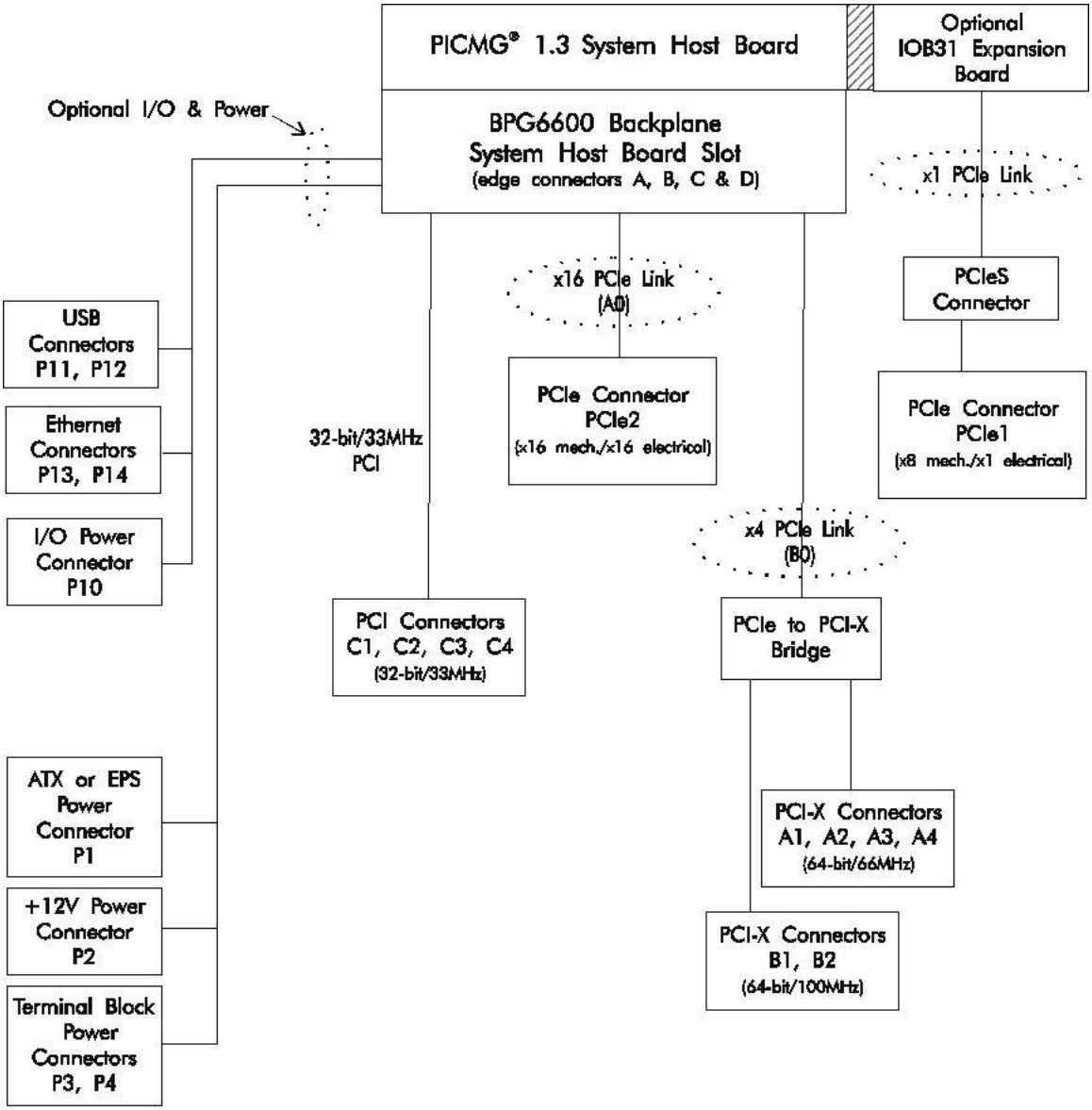
USB and Ethernet functionality on the BPG6600 is dependent on the SHB providing I/O capability to edge connector C of the backplane. In order to take advantage of these I/O features, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

The backplane has a power connector (P1) which can accommodate either ATX or EPS power. A +12V power connector (P2) is provided for routing auxiliary power to the SHB's edge connectors, eliminating the need for auxiliary power connections on the system host board. The BPG6600 also has two extended-current terminal block connectors which provide additional power capacity for power-intensive applications -- up to 80 Amps of +12V, 80 Amps of +3.3V and 40 Amps of +5V.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

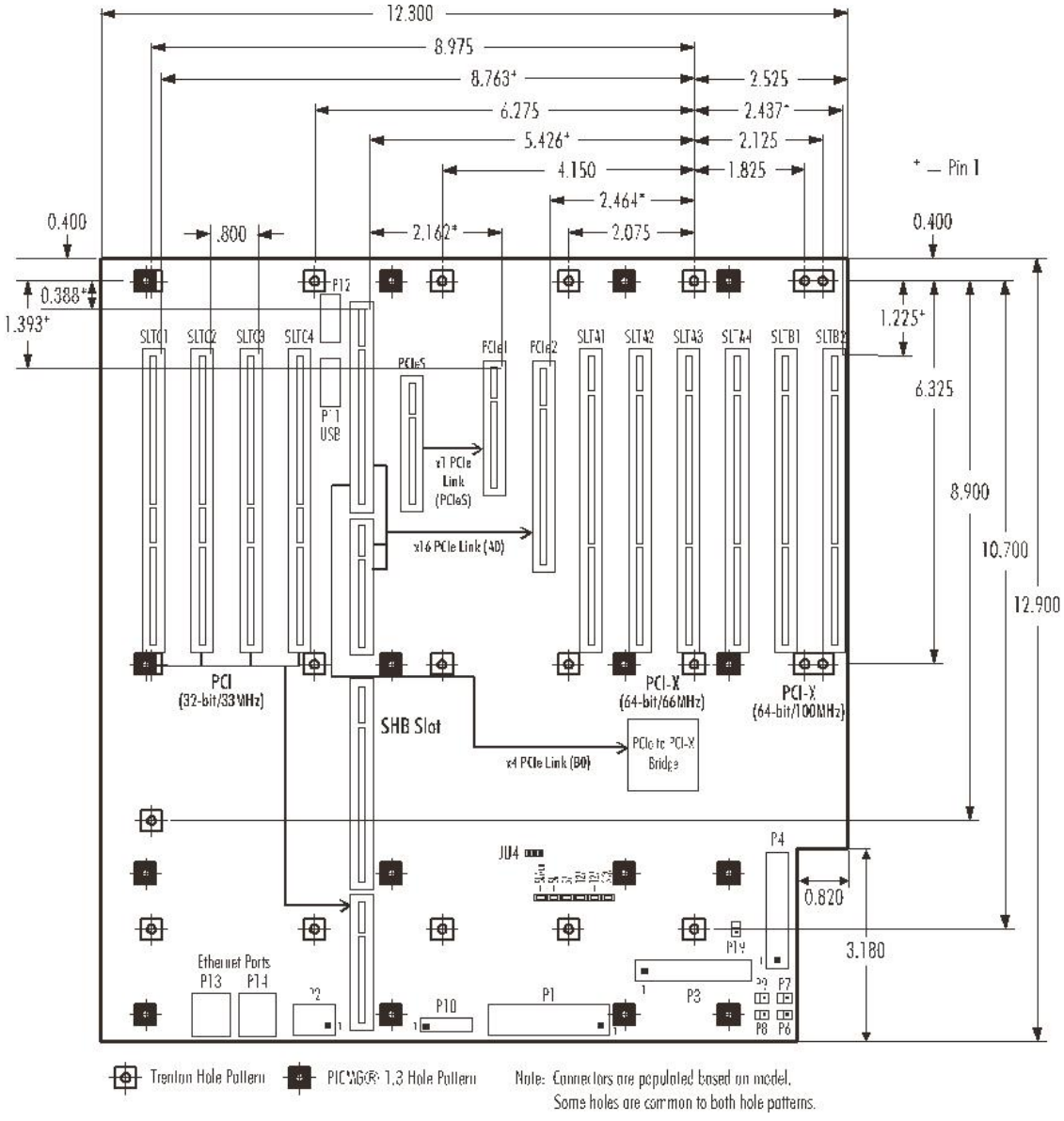
Models with other power configurations may be available. Contact Trenton Technology for more information.

6600-000 BPG6600 BLOCK DIAGRAM



6600-000 BPG6600 DIMENSIONAL DRAWINGS

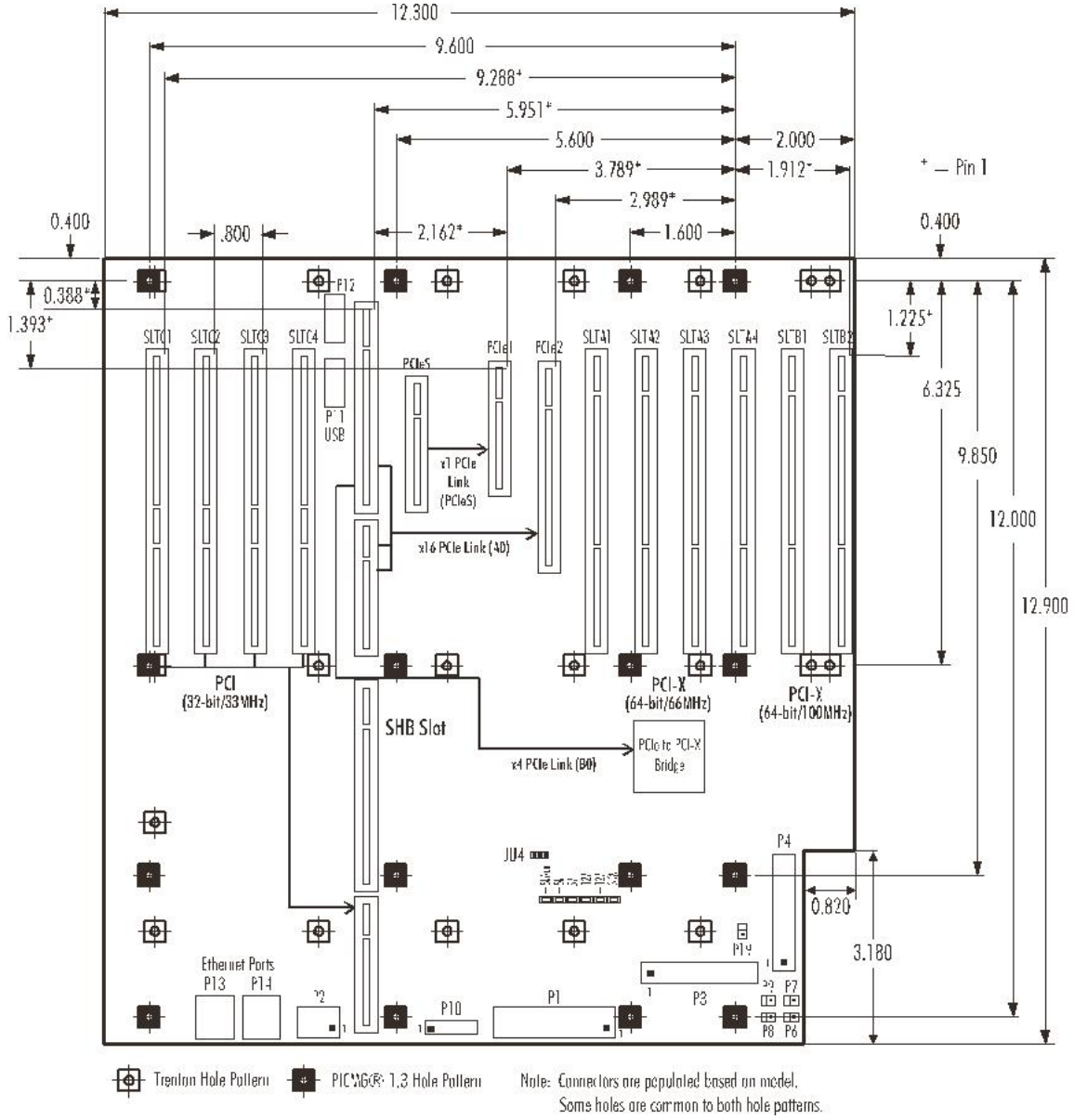
Trenton 14-Slot Hole Pattern



PCB thickness .080”
Mounting holes .156” diameter
Connector spacing .800” centers

6600-000 BPG6600 DIMENSIONAL DRAWINGS

PICMG® 1.3 14-Slot Hole Pattern



PCB thickness .080”
Mounting holes .156” diameter
Connector spacing .800” centers

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

BPG6600 CONNECTORS

The connectors available on the BPG6600 vary depending on the version of the backplane you have. Connectors for the 6600-004 (-EPS) and 6600-007 (-CRA) are defined below.

6600-004 BPG6600-EPS CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin dual row mini fit JR, Molex #39-29-6248

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

6600-004 BPG6600-EPS CONNECTORS (CONTINUED)

P2 - +12V Power Connector

8 pin mini fit JR, Amp #1586037-8

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P3 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0

20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	Gnd
4	Gnd
5	Gnd
6	Gnd
7	+12V
8	+12V
9	+12V
10	+12V

P4 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0

20 Amps per circuit

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	+3.3V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	Gnd

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

6600-004 BPG6600-EPS CONNECTORS (CONTINUED)

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin dual row header, Molex #87831-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	+5VAUX_IN
17	Gnd	18	+5VAUX_IN
19	Gnd	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801

(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

6600-004 BPG6600-EPS CONNECTORS (CONTINUED)

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RJ-45 connector, Molex #85508-0001

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RJ-45 connector, Molex #85508-0001

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - System Management Bus Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

6600-007 BPG6600-CRA CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin right angle dual row mini fit JR, Amp #1-794516-1

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P2 - +12V Power Connector

8 pin right angle mini fit JR, Molex #39-30-0080

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P3 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0

20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	Gnd
4	Gnd
5	Gnd
6	Gnd
7	+12V
8	+12V
9	+12V
10	+12V

6600-007 BPG6600-CRA CONNECTORS (CONTINUED)

P4 - Terminal Block Connector

10 position terminal block, Amp #1-796949-0
20 Amps per circuit

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	+3.3V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	Gnd

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

6600-007 BPG6600-CRA CONNECTORS (CONTINUED)

P10 - I/O Power Connector

20 pin dual row header, Molex #87831-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	+5VAUX_IN
17	Gnd	18	+5VAUX_IN
19	Gnd	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RJ-45 connector, Molex #85508-0001

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

6600-007 BPG6600-CRA CONNECTORS (CONTINUED)

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RJ-45 connector, Molex #85508-0001

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - System Management Bus Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SMB Clock
2	SMB Data

6615-000 BPG6615

The BPG6615 is a graphics-class PICMG-compatible backplane which is a six-layer .080" thick PCB. It is PICMG® 1.3 compliant and supports Trenton and PICMG® 1.3 14-slot (64-bit) hole patterns.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has five PCI Express slots (PCIe2 through PCIe6) which provide the mechanical connections between the PCI Express option cards and the SHB. PCIe2 is a x16 mechanical driven by a x16 PCI Express link directly from a graphics class SHB and is ideal for high-end graphics cards. It is capable of supporting x16, x8, x4 and x1 PCI Express option cards. PCIe3 through PCIe6 are x8 mechanical slots and each slot is deiven by a x4 PCI Express link from the PCI Express fan-out switch. The fan-out switch is driven by a x4 PCI Express link from the graphics-class SHB.

In addition, the BPG6615 has six PCI-X slots. The six PCI-X slots on the BPG6615 are connected to the SHB via a x4 PCI Express link delivered from the PCI Express fan out switch to the PCI Express-to-PCI-X bridge chip. The bridge chip provides a 64-bit/66MHz PCI-X channel to support option card slots SLTA1 through SLTA4 and a 64-bit/100MHz PCI-X channel to support slots SLTB1 and SLTB2. These slots support PCI-X and universal PCI option cards i.e., 5V/3.3V combo or 3.3V only. The bridge chip will throttle-down the bus interface speeds to match any universal PCI or PCI-X card with an interface bus speed less than 66MHz or 100MHz.

NOTE: The 64-bit/66MHz PCI-X slots enable 66MHz PCI-X option cards to run at 66MHz. 66MHz PCI option cards will function in these slots but may only operate at 33MHz due to the differences between a PCI and PCI-X bus.

The BPG6615 supports the optional Ethernet routing feature of the SHB Express specification and provides two 10/100/1000Base-T Ethernet RJ-45 connectors. It also has two USB 2.0 headers which are capable of supporting up to four USB 2.0 ports on the backplane.

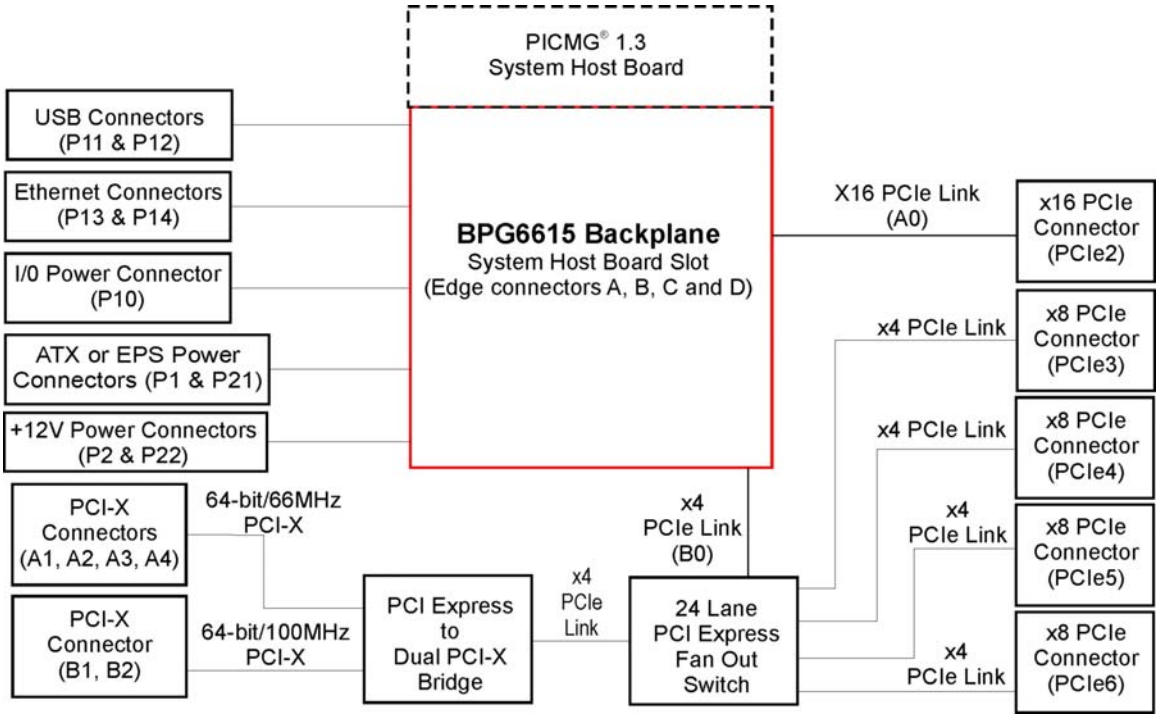
USB and Ethernet functionality on the BPG6615 is dependent on the SHB providing I/O capability to edge connector C of the backplane. In order to take advantage of these I/O features, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

The backplane has both right angle and horizontal power connectors which can accommodate either ATX or EPS power. Two +12V power connectors, right angle and horizontal, are provided for routing auxiliary power to the SHB's edge connectors, eliminating the need for auxiliary power connections on the system host board. The BPG6615 also has two extended-current terminal block connectors which provide additional power capacity for power-intensive applications -- up to 80 Amps of +12V, 120 Amps of +3.3V and 80 Amps of +5V.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

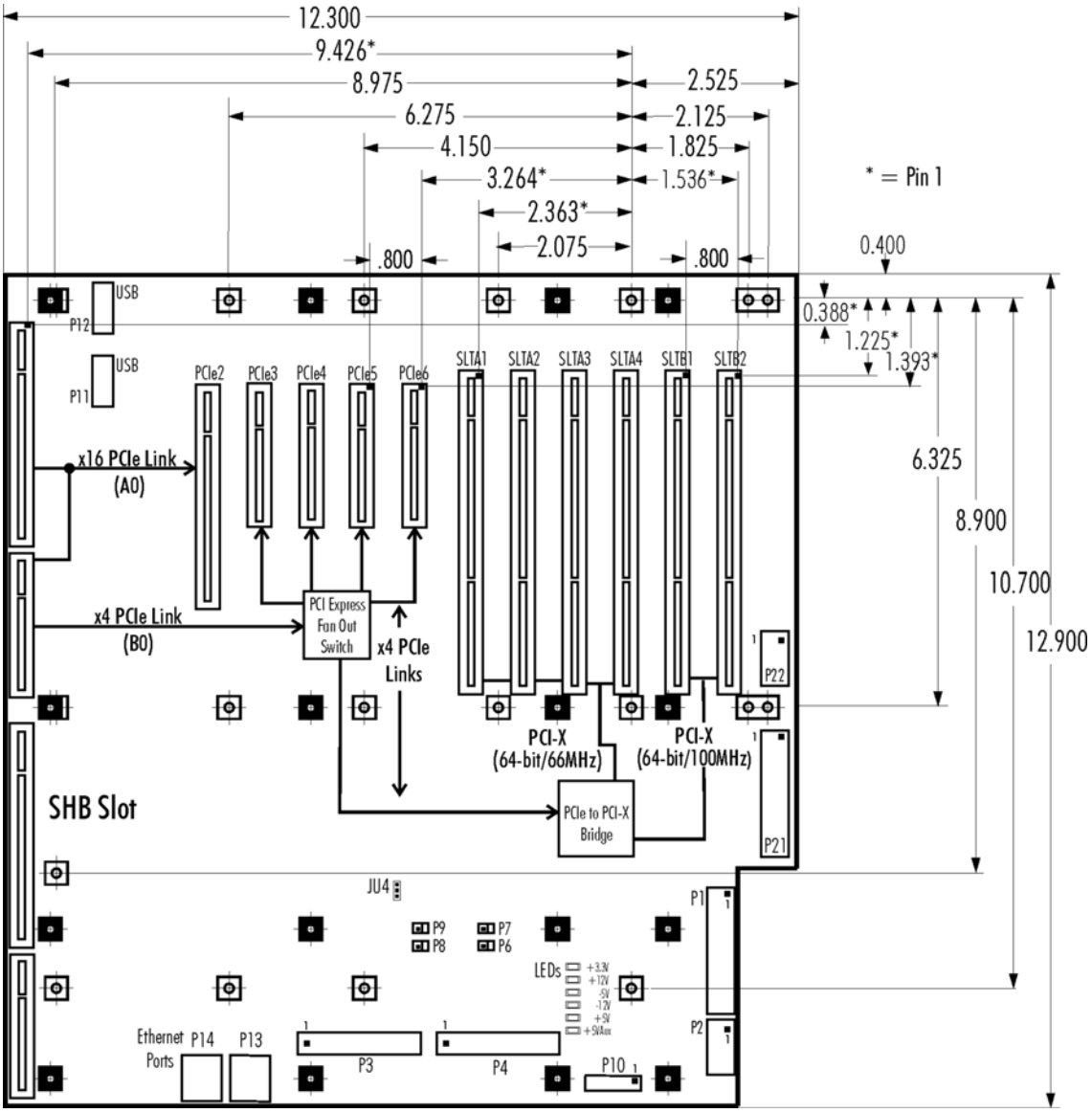
Models with other power configurations may be available. Contact Trenton Technology for more information.

6615-000 BPG6615 BLOCK DIAGRAM



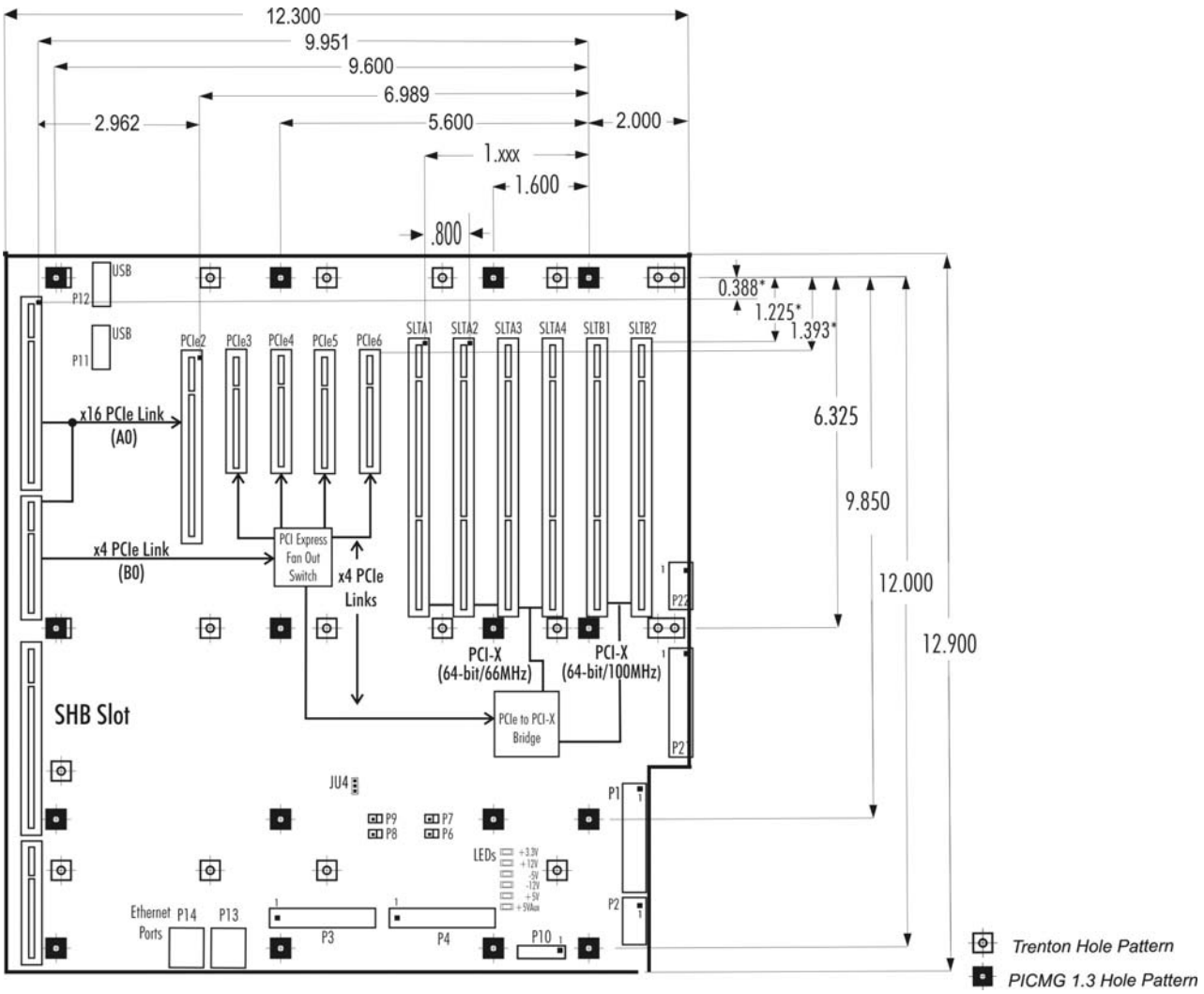
6615-000 BPG6615 DIMENSIONAL DRAWING

Trenton Hole Pattern



6615-000 BPG6615 DIMENSIONAL DRAWING

PICMG 1.3 Hole Pattern



*=Pin 1

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "TOP" and "BOTTOM" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the TOP if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the BOTTOM if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

6615-007 BPG6615 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin right angle dual row, Molex #39-30-1240

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P2 - +12V Power Connector

8 pin right angle dual row, Molex #39-30-0080

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

6615-007 BPG6615 CONNECTORS (CONTINUED)

P3 - Terminal Block Connector

10 position terminal block, Phoenix Contract Inc., 19-35-24-2
20 Amps per circuit

Pin	Signal
1	+3.3V
2	+3.3V
3	+3.3V
4	+3.3V
5	Gnd
6	Gnd
7	Gnd
8	Gnd
9	Gnd
10	Gnd

P4 - Terminal Block Connector

10 position terminal block, Phoenix Contract Inc., 19-35-24-2
20 Amps per circuit

Pin	Signal
1	+5V
2	+5V
3	Gnd
4	Gnd
5	Gnd
6	Gnd
7	Gnd
8	+12V
9	+12V
10	+12V

P6 - Power-On Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	PWRGD
2	Gnd

6615-007 BPG6615 CONNECTORS (CONTINUED)

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	5VAUX
17	GND	18	5VAUX
19	GND	20	-12V

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin shielded RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

6615-007 BPG6615 CONNECTORS (CONTINUED)

P14 - 10/100/1000Base-T Ethernet Connector - LAN 1

8 pin shielded RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - SMBUS Connector

2 pin single row header, Amp #640456-2

Pin	Signal
1	SMBUS
2	Gnd

P21 - EPS Power Connector

24 pin vertical dual row, Molex #44206-0007

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P22 - +12V Power Connector

8 pin vertical dual row, Molex #44206-0005

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

6714-000 BPG6714

The BPG6714 is a PICMG® 1.3 compliant, small form factor, graphics-class backplane made up of a six-layer .062" thick PCB.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has two PCI Express slots (PCIe1 and PCIe3) which provide the mechanical connections between the PCI Express option cards and the SHB.

PCIe1 can mechanically support x8, x4 and x1 PCI Exress option cards. PCIe1 uses the PCIe link provided by the SHB via a Trenton IOB31 I/O expansion board. The IOB31, when attached to a MCG-series SHB, provides a x4 PCIe link from the SHB to the backplane's PCIeS slot. A TML or T4L may also be used. These SHBs will provide a x1 PCI Express link to the BPG6714 backplane's PCIeS slot via an IOB31 module.

PCIe3 is a x16 mechanical slot that is driven by a x16PCI Express link (A0) from the SHB. This slot Is designed to electrically and mechanically support high-end PCI Express graphics and video cards that use a x16 PCI Express link to communicate to the SHB.

In addition, the BPG6714 has three PCI-X slots (SLTA1, SLTB1 and SLTB2). These are connected to the SHB via a x4 PCI Express link (B0) via a PCI Express-to-PCI-X bridge chip. The bridge chips support SLTA1 with a 64-bit/133MHz PCI-X interface and SLTB1 and SLTB2 with a 64-bit/100MHz PCI-X interface.

The BPG6714 supports the optional Ethernet routing feature of the SHB Express specification and provides one 10/100/1000Base-T Ethernet RJ-45 connectors. It also has two USB 2.0 headers which are capable of supporting up to four USB 2.0 ports on the backplane.

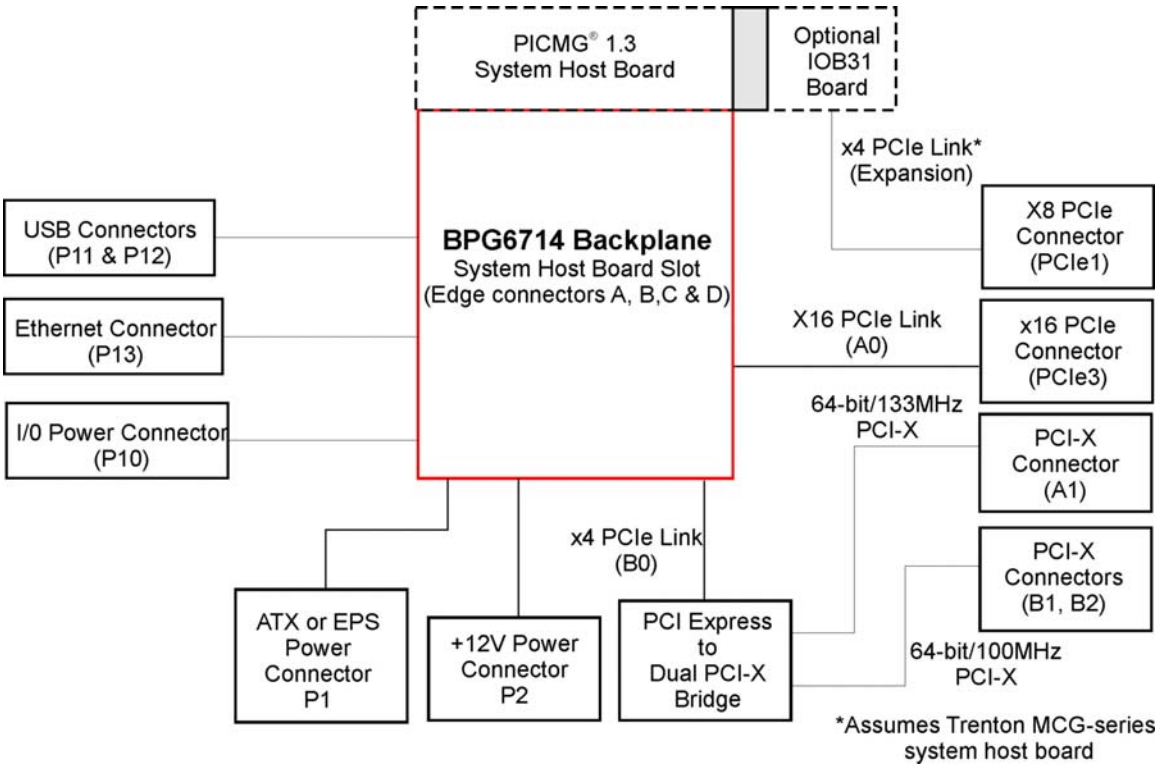
NOTE: USB and Ethernet functionality on the BPG6714 is dependent on the SHB providing I/O capability to edge connector C of the backplane. In order to take advantage of these I/O features, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3.*

The standard BPG6714 backplane is available with a low-profile right-angle power connector sutiable for use with either an ATX or EPS power supply. An optional BGP6714 is available with straight in or vertical power connectors. Using straight-in power connectors may interfere with a full-length option card placed in the SLTB1 slot.

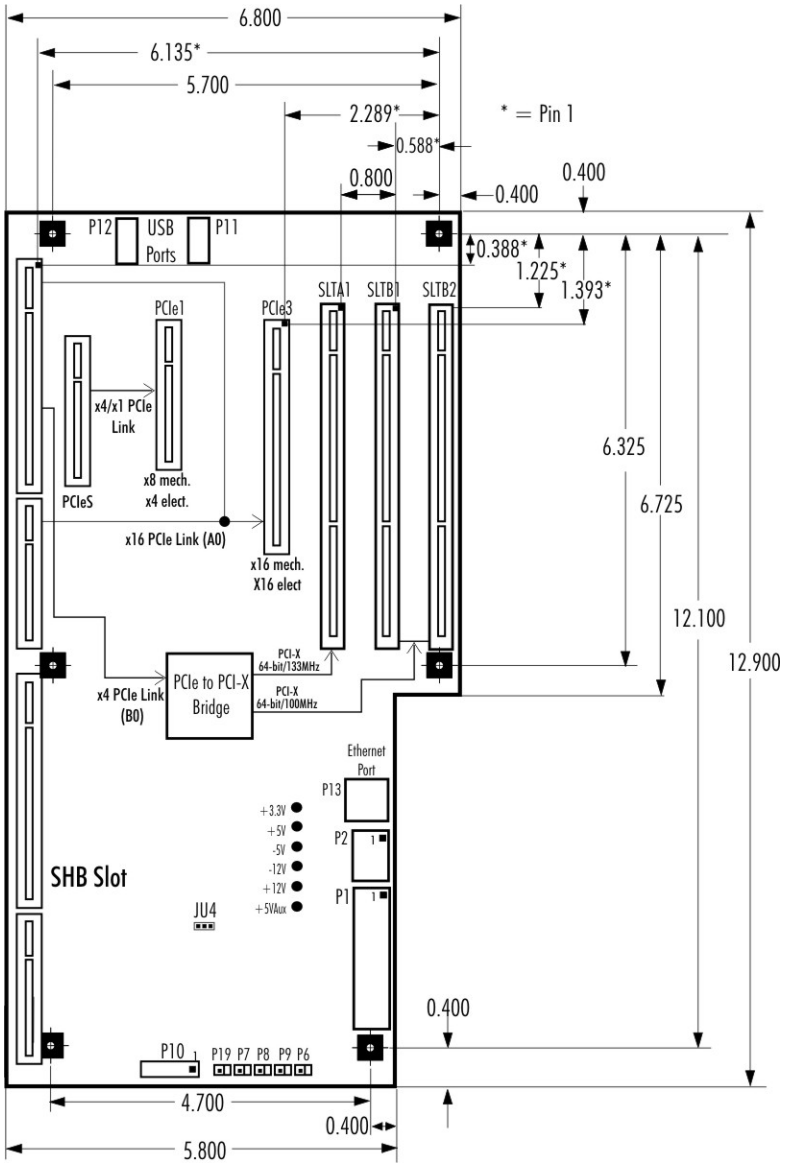
CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

Models with other power configurations may be available. Contact Trenton Technology for more information.

6714-000 BPG6714 BLOCK DIAGRAM



6714-000 BPG6714 DIMENSIONAL DRAWING



**IOB31 required to provide PCI Express link to PCIe1 slot*
***Optional USB, Ethernet connectivity provided by PICMG 1.3 System Host Board. Not all SHBs support this capability.*
Nominal PCB thickness .062"
Connector spacing .800" centers
To find the center of a PCI-X/PCI option card connector add 0.150" to the pin 1 location dimension.
To find the center of the SHB or a PCI Express option card connector add 0.049" to the pin 1 location dimension.
Mounting holes .156" diameter
All dimensions are inches.

Trenton Hole Pattern

PICMG 1.3 Hole Pattern

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

6714-007 BPG6714 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin right angle dual row, Molex #39-30-1240

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

6714-007 BPG6714 CONNECTORS (CONTINUED)

P2 - +12V Power Connector

8 pin right angle dual row, Molex #39-30-0080

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P6 - Power-On Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRGD
2	Gnd

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	5VAUX
17	GND	18	5VAUX
19	GND	20	-12V

6714-007 BPG6714 CONNECTORS (CONTINUED)

P11 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1

P12 - Universal Serial Bus (USB) Connector

8 pin dual row header, Molex #702-46-0801
(+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB2	2	+5V-USB3
3	USB2-	4	USB3-
5	USB2+	6	USB3+
7	Gnd-USB2	8	Gnd-USB3

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0

8 pin right angle shielded RJ-45 connector, Molex #43202-8919

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - SMBUS Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SMBUS
2	Gnd

This page intentionally left blank.

Chapter 5 - Multiple SHB Segment Backplanes

6605-000 BP6FS6605

The BP6FS6605 is a six-segment, PICMG-compatible backplane which is a six-layer .080" thick PCB. The six SHB segments are flexible enough to be ordered in either a graphics-class or server-class configuration. It is PICMG® 1.3 compliant and supports Trenton and PICMG® 1.3 20-slot mounting hole patterns.

In a graphics-class configuration of the BP6FS6605, the SHB slot in each backplane segment supports a graphics-class PICMG 1.3 system host board such as Trenton's TML. Each graphics-class SHB segment supports the segment's x16 PCI Express (PCIe) mechanical slot with a x16 PCIe electrical link from the SHB. There is one x16 PCIe mechanical slot for each SHB segment: PCIe1-2, PCIe2-2, PCIe3-2, PCIe4-1, PCIe5-1 and PCIe6-1.

In a server-class configuration of the BP6FS6605, the SHB slot in each backplane segment supports server-class PICMG 1.3 system host boards such as the Trenton SLT or SLI. Each server-class SHB segment supports the x16 PCI Express (PCIe) mechanical slot with a x8 PCIe electrical link from the SHB.

SHB segments A1, A2 and A3 also feature a x8 PCIe mechanical slot. These slots are labeled PCIe1-1, PCIe2-1 and PCIe3-1 and are driven by an SHB's x4 PCI Express link in both graphics-class and server-class configurations of the backplane.

Trenton's BP6FS6605 backplane is available with an optional Ethernet fabric to enable the SHBs in each segment to share data and communicate information to and from the system host via the backplane's Ethernet hub port. The backplane's optional Ethernet hub switch makes this functionality possible. The Ethernet hub switch controls the SHB-to-SHB communication and the SHB's communication to the host system via the 10/100Base-T Ethernet port interface. This optional backplane capability requires that the SHB support the optional Ethernet interface routing to SHB edge connector C as defined in the PICMG 1.3 or SHB Express specification. The Ethernet fabric on the BP6FS6605 backplane enables many system advantages in applications that require cluster computing.

Each backplane segment provides soft control power circuitry to control the power-up and power-down sequences of each SHB segment. Connecting an independent power source to each segment maximizes the power control aspect of each backplane segment. The BP6FS6605 backplane allows segments to be powered individually or grouped together for the purpose of being powered by a single power source. Care must be used when grouping segments together to ensure that adequate power is provided and the desired power sequences are controlled.

The BP6FS6605 backplane supports two backplane connector option types: ATX/EPS and terminal blocks.

In the ATX/EPS configuration, each SHB segment is usually powered by a separate ATX or EPS power supply. A 24-pin vertical power connector in each SHB segment provides the interface to the segment's power supply. Each segment also includes a +12V auxiliary power connector for routing the auxiliary power directly to the SHB's edge connectors. This new capability of PICMG 1.3 compliant SHBs and backplanes eliminates the need for auxiliary power connections on the system host board. The BP6FS6605 backplane power connectors used in the standalone configuration are suitable for use with either an ATX or EPS power supply.

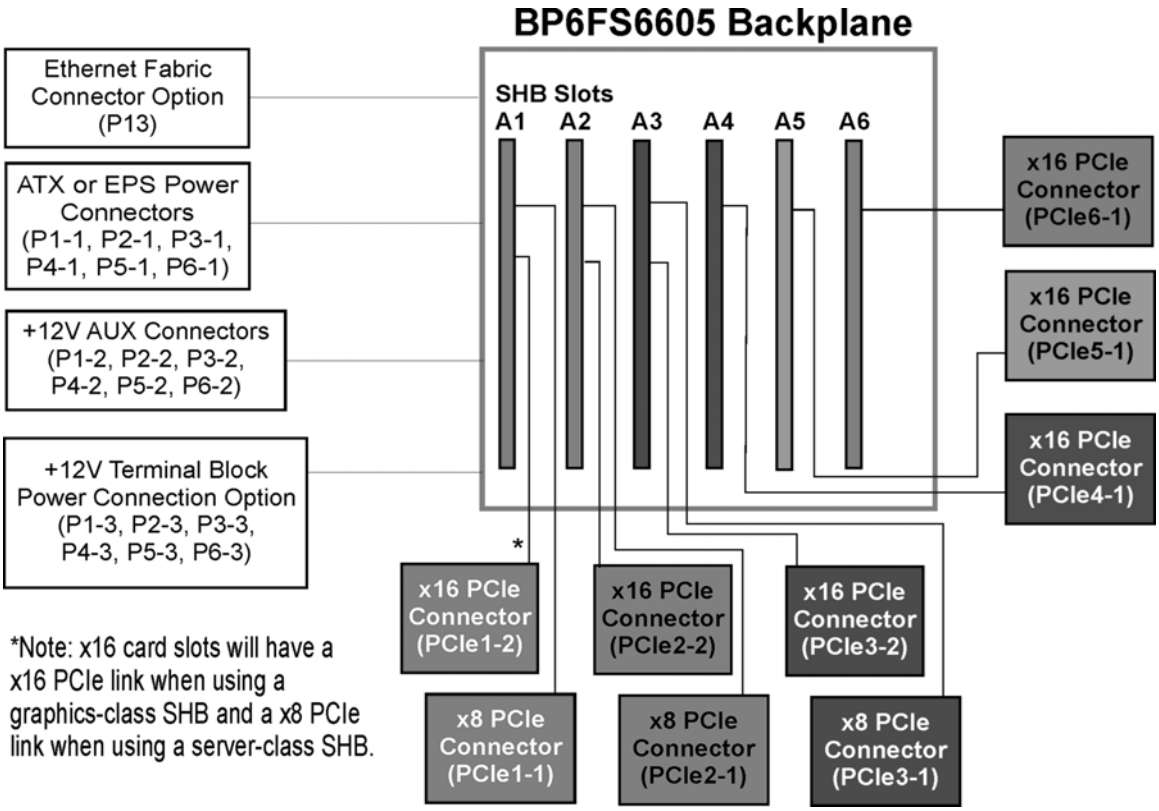
The terminal block connectors enable each SHB segment or multiple segments to be powered by a +12V power source. The voltage regulator circuits in each SHB segment provide all of the required voltage levels for the SHB and option card slots. Using the terminal blocks is the recommended method for grouping together segments in order to drive multiple segments with a common power supply. (Note:

grouping segments with the standard ATX/EPS power connectors is also allowed, but Trenton recommends using the terminal blocks for this type of multiple SHB segment power connection.) Each segment's four-position terminal block provides additional power capacity and up to 80 Amps of +12V.

CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; “green” indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

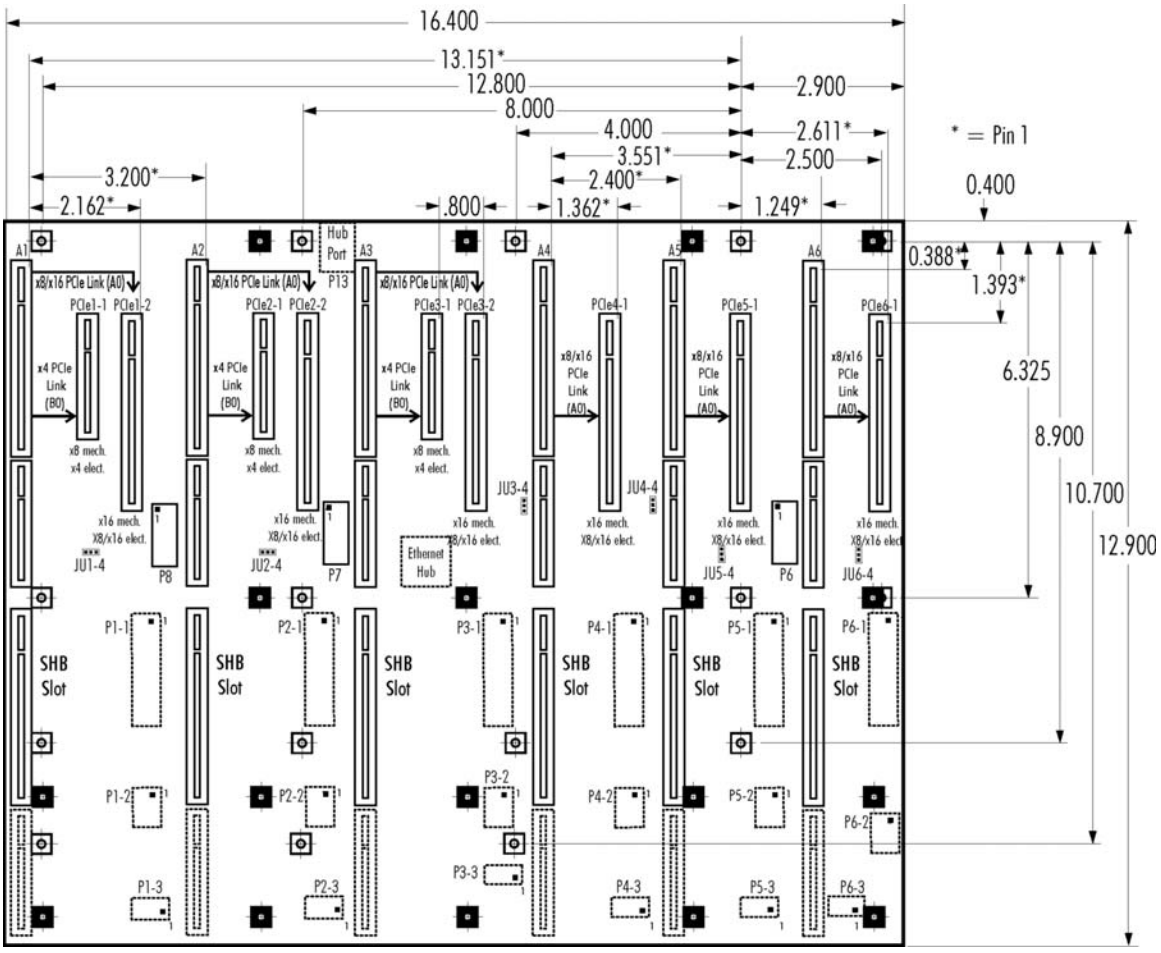
Models with other power configurations may be available. Contact Trenton Technology for more information.

6605-000 BP6FS66055 BLOCK DIAGRAM



6605-000 BP6FS6605 DIMENSIONAL DRAWING

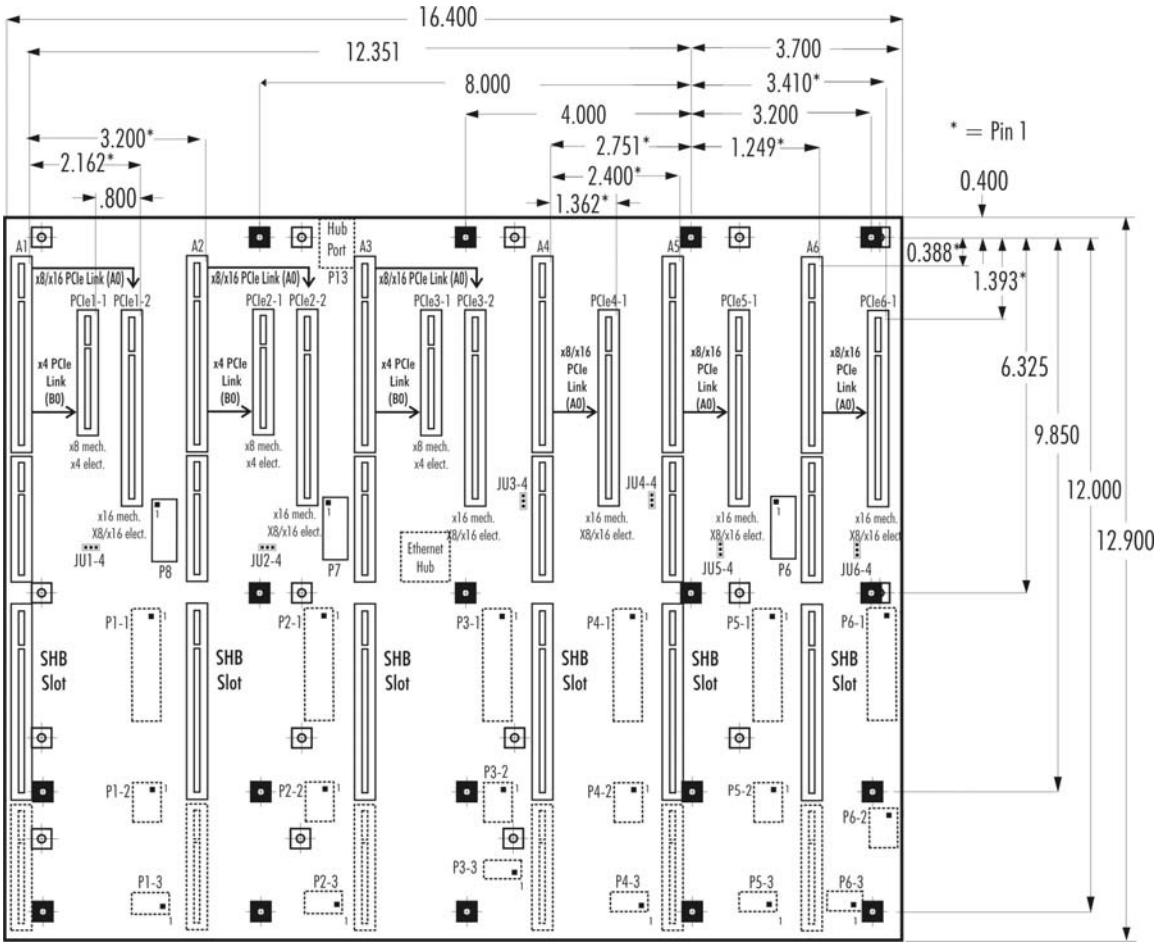
Trenton Hole Pattern



Note: Connectors and components on the layout drawings shown in dotted lines may or may not be populated on your specific model of the BP6FS66005 backplane. Refer to Backplane Configuration Table.

6605-000 BP6FS6605 DIMENSIONAL DRAWING

PICMG 1.3 Hole Pattern



Note: Connectors and components on the layout drawings shown in dotted lines may or may not be populated on your specific model of the BP6FS66005 backplane. Refer to Backplane Configuration Table.

6605-000 BP6FS6605 BACKPLANE CONFIGURATION TABLE

Model#	Model Name & Type	SHB Connector D	ATX/EPS Connectors P1-1 P2-1 P3-1 P4-1 P5-1 P6-1	+12V Aux Connectors P1-2 P2-2 P3-2 P4-2 P5-2 P6-2	+12V Terminal Blocks P1-3 P2-3 P3-3 P4-3 P5-3 P6-3	Ethernet Hub	Ethernet Hub Port P13
6605-005	BP6FS6605-SCSV, Server-class, Standalone, Vertical ATX/EPS connectors	No	Yes	Yes	No	No	No
6605-016	BP6FS6605-SCST, Server-class, Standalone, Terminal Block connectors	No	No	No	Yes	No	No
6605-025	BP6FS6605-SCEV, Server-class, Ethernet, Vertical ATX/EPS connectors	No	Yes	Yes	No	Yes*	Yes*
6605-036	BP6FS6605-SCET, Server-class, Ethernet, Terminal Block connectors	No	No	No	Yes	Yes*	Yes*
6605-105	BP6FS6605-GCSV, Graphics-class, Standalone, Vertical ATX/EPS connectors	Yes	Yes	Yes	No	No	No
6605-116	BP6FS6605-GCST, Graphics-class, Standalone, Terminal Block connectors	Yes	No	No	Yes	No	No
6605-125	BP6FS6605-GCEV,Graphics-class, Ethernet, Vertical ATX/EPS connectors	Yes	Yes	Yes	No	Yes	Yes
6605-136	BP6FS6605-GCET, Graphics-class, Ethernet, Terminal Block connectors	Yes	No	No	Yes	Yes	Yes

*TRENTON SLT/SLI SYSTEM HOST BOARDS DO NOT SUPPORT THIS FUNCTION ON THE BACKPLANE

CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post) in SHB segments 1 and 2, "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the SHB's I/O plate(s) at the top end of the backplane.

NOTE: For the two-position jumper (3-post) in SHB segments 3, 4, 5 and 6, "TOP" and "BOTTOM" refer to positioning when the backplane is viewed with the SHB's I/O plate(s) at the top end of the backplane.

Jumper	Description
JU4, 1-2	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. * Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies.
JU4, 3-6	**+5V Auxiliary Voltage** Install on the TOP if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. * Install on the BOTTOM if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies.

6605-000 BP6FS6605 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1, 1-6 - EPS Power Connector

24 pin vertical dual row, Molex #44206-0007

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P2, 1-6 - +12V Power Connector

8 pin vertical dual row, Molex #44206-0005

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P3, 1-6 - Terminal Block Connector

4 position terminal block, AMP, #796949-4

20 Amps per circuit

Pin	Signal
1	+12V
2	+12V
3	Gnd
4	Gnd

P6 - Power-On Connector

14 pin dual row connector, 3M, #N2514-6002RB

Pin	Signal	Pin	Signal
1	PSON# - 1	2	Gnd - 1
3	PSON# - 2	4	Gnd - 2
5	PSON# - 3	6	Gnd - 3
7	PSON# - 4	8	Gnd - 4
9	PSON# - 5	10	Gnd - 5
11	PSON# - 6	12	Gnd - 6
13	NC	14	NC

6605-000 BP6FS6605 CONNECTORS (CONTINUED)

P7 - Power Button Connector

14 pin dual row connector, 3M, #N2514-6002RB

Pin	Signal	Pin	Signal
1	PWRBT# - 1	2	Gnd - 1
3	PWRBT# - 2	4	Gnd - 2
5	PWRBT# - 3	6	Gnd - 3
7	PWRBT# - 4	8	Gnd - 4
9	PWRBT# - 5	10	Gnd - 5
11	PWRBT# - 6	12	Gnd - 6
13	NC	14	NC

P8 - Reset Connector

14 pin dual row connector, 3M, #N2514-6002RB

Pin	Signal	Pin	Signal
1	SHB_RST# - 1	2	Gnd - 1
3	SHB_RST# - 2	4	Gnd - 2
5	SHB_RST# - 3	6	Gnd - 3
7	SHB_RST# - 4	8	Gnd - 4
9	SHB_RST# - 5	10	Gnd - 5
11	SHB_RST# - 6	12	Gnd - 6
13	NC	14	NC

P13 - 10/100 Base-T Ethernet Connector – Backplane Hub Port

8 pin right angle shielded RJ-45 connector, Pulse, #J0035D21BNL

Pin	Signal
1	RXD-
2	RXD+
3	RCI
4	RC
5	TC
6	TCI
7	TXD-
8	TXD+

6890-000 BP4FS6890

The BP4FS6890 is a four-segment PICMG 1.3 backplane built on a .080" thick PCB. The four SHB segments may be factory configured to support PICMG 1.3 graphics or server-class system implementations. This 20-slot form factor backplane is fully compliant with the PICMG 1.3 (SHB Express®) specification and supports both the Trenton and PICMG 1.3 mounting hole patterns.

In a server-class configuration of the BP4FS6890, the SHB slot in each backplane segment supports server-class PICMG 1.3 system host boards such as the Trenton MCXT, MCXT-E, MCXI, SLT, SLI, NLT or NLI. Each server-class SHB segment supports two x16 PCI Express (PCIe) mechanical slots with x8 PCIe electrical links directly from the segment's single board computer. These option card slots are numbered: PCIe1-2, PCIe2-2, PCIe3-2, PCIe4-2, PCIe1-3, PCIe2-3, PCIe3-3 and PCIe4-3. SHB option card slot positions PCIe1-1, PCIe2-1, PCIe3-1 and PCIe4-1 are x8 PCIe mechanical card slots and each slot is driven with a x4 PCIe electrical link.

In a graphics-class configuration of the BP4FS6890 the SHB slot in each backplane segment supports a graphics-class PICMG 1.3 system host board such as Trenton's TQ9, MCGT, MCGT-E, MCGI, TML or T4L. Each graphics-class SHB segment supports the x16 PCI Express (PCIe) mechanical slot that is farthest from the segment's SHB slot with a x16 PCIe electrical link. In each SHB segment, the x16 PCIe mechanical slot with the x16 electrical link directly from the single board computer is numbered: PCIe1-3, PCIe2-3, PCIe3-3 or PCIe4-3. The x16 mechanical slot that is closest to a segment's SHB is numbered PCIe1-2, PCIe2-2, PCIe3-2 or PCIe4-2, and this card slot is driven with a x4 PCIe link from the single board computer. SHB option card slot locations PCIe1-1, PCIe2-1, PCIe3-1 and PCIe4-1 are silk screened on the backplane, but are blank connector positions in the BP4FS6890 graphic-class backplane configuration.

Trenton's BP4FS6890 backplane is available with an optional Ethernet fabric to enable the SHBs in each segment to share data and communicate information to and from the system host via the backplane's Ethernet hub port. The backplane's optional Ethernet hub switch makes this functionality possible. The Ethernet hub switch controls the SHB-to-SHB communication and the SHB's communication to the host system via the backplane's 10/100/1000Base-T Ethernet port. This optional backplane capability requires that the SHBs support the optional Ethernet interface routing to SHB edge connector C as defined in the PICMG 1.3 or SHB Express specification. The Ethernet fabric on the BP4FS6890 backplane enables many system advantages in applications that require cluster computing.

The BP4FS6890 backplane supports two backplane power connector options: ATX/EPS or terminal blocks.

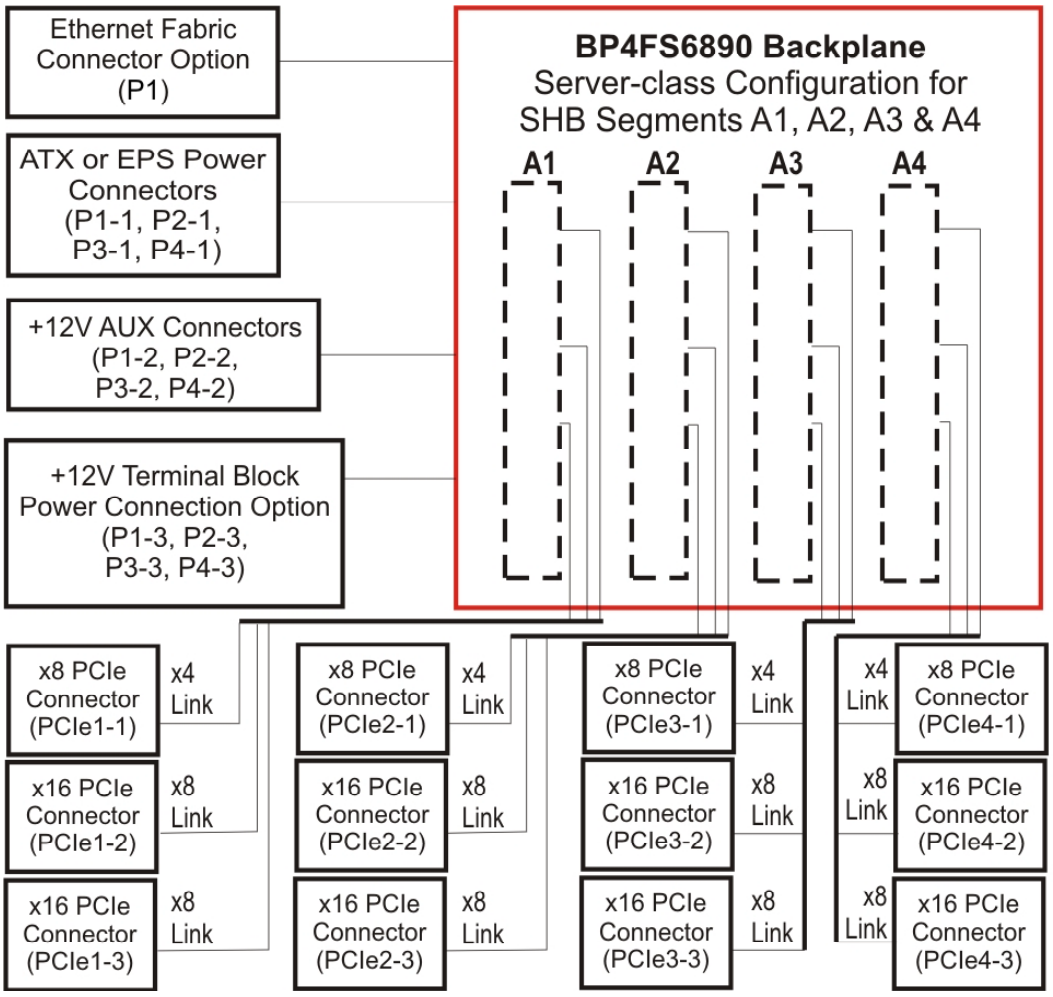
In the ATX/EPS configuration, each SHB segment is usually powered by a separate ATX or EPS power supply. A 24-pin right-angle power connector in each SHB segment provides the interface to the segment's power supply. Each segment also includes an eight-position, +12V AUX, right-angle power connector for routing the auxiliary power directly to the SHB's edge connectors. This feature of PICMG 1.3 compliant SHBs and backplanes eliminates the need for auxiliary power connections on the system host board. The BP4FS6809 backplane power connectors used in the standalone configuration are suitable for use with either an ATX or EPS power supply.

The six-position terminal block connector option enables each SHB segment or multiple segments to be powered by a +12V power source. The voltage regulator circuits in each SHB segment provides all of the required voltage levels for the SHB and option card slots. Using the terminal blocks is the recommended method for grouping together segments with a common power supply. (Note: grouping segments with the standard ATX/EPS power connectors is allowed, but Trenton recommends using the terminal blocks for this type of multiple SHB segment power connection.)

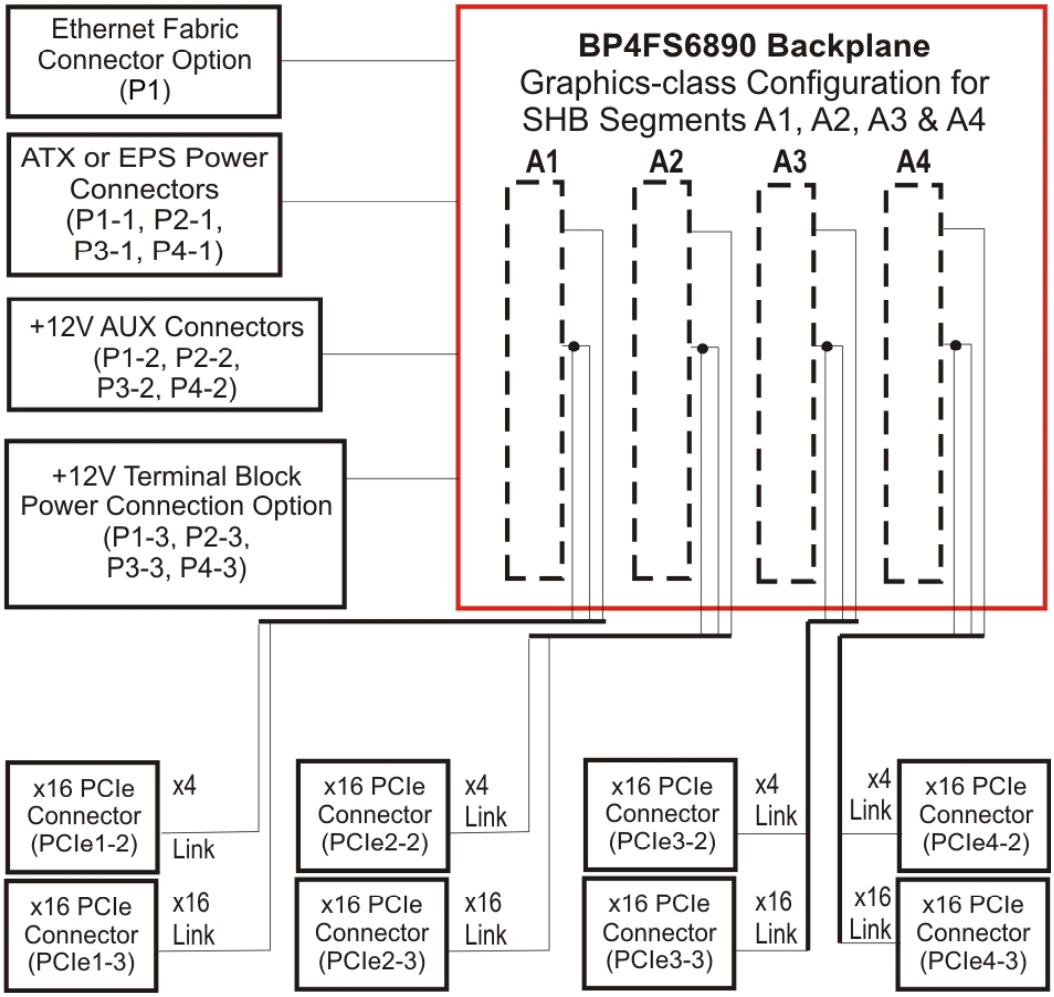
CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

Models with other power configurations may be available. Contact Trenton Technology for more information.

6890-000 BP4FS6890 SERVER-CLASS BLOCK DIAGRAM

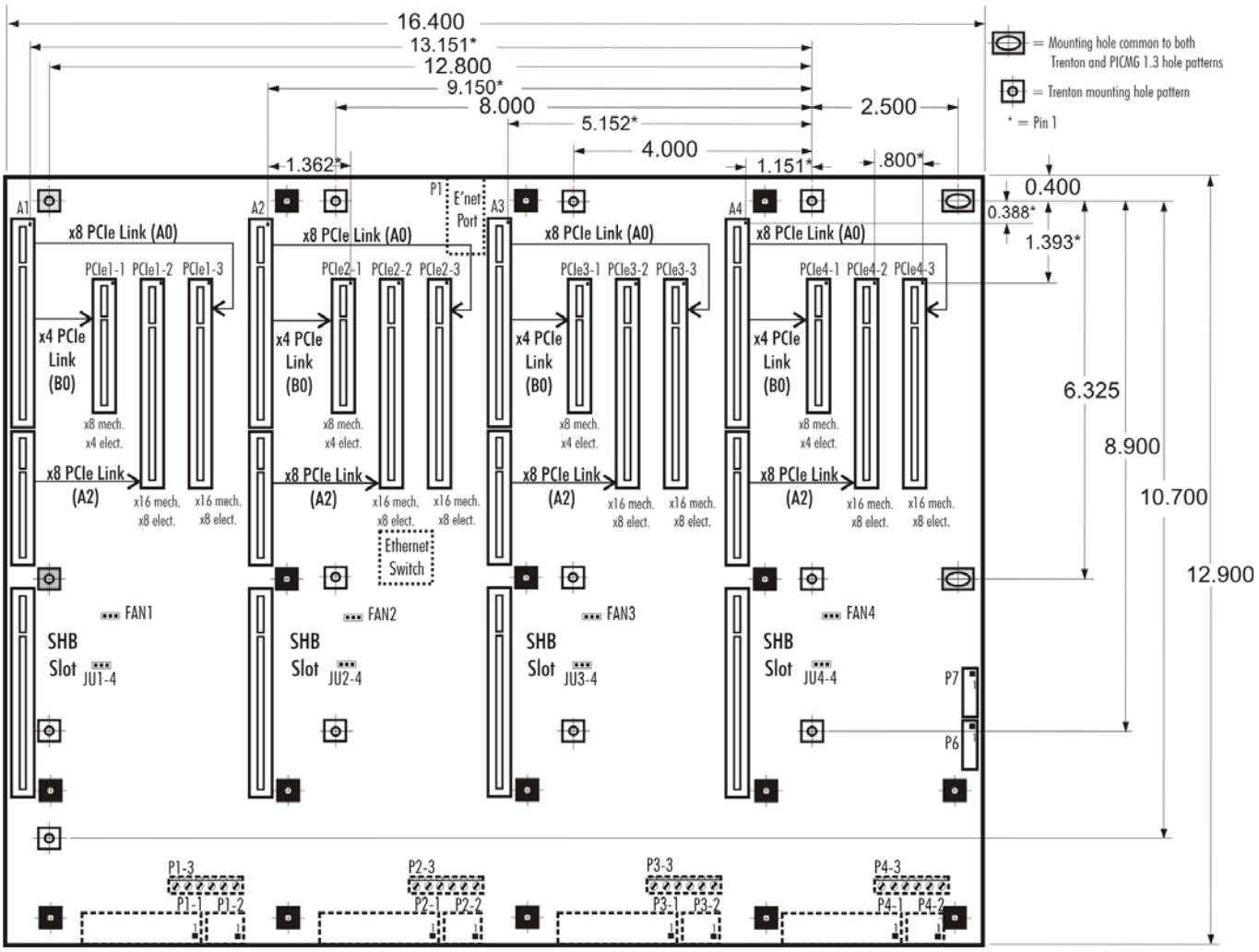


6890-000 BP4FS6890 GRAPHICS-CLASS BLOCK DIAGRAM



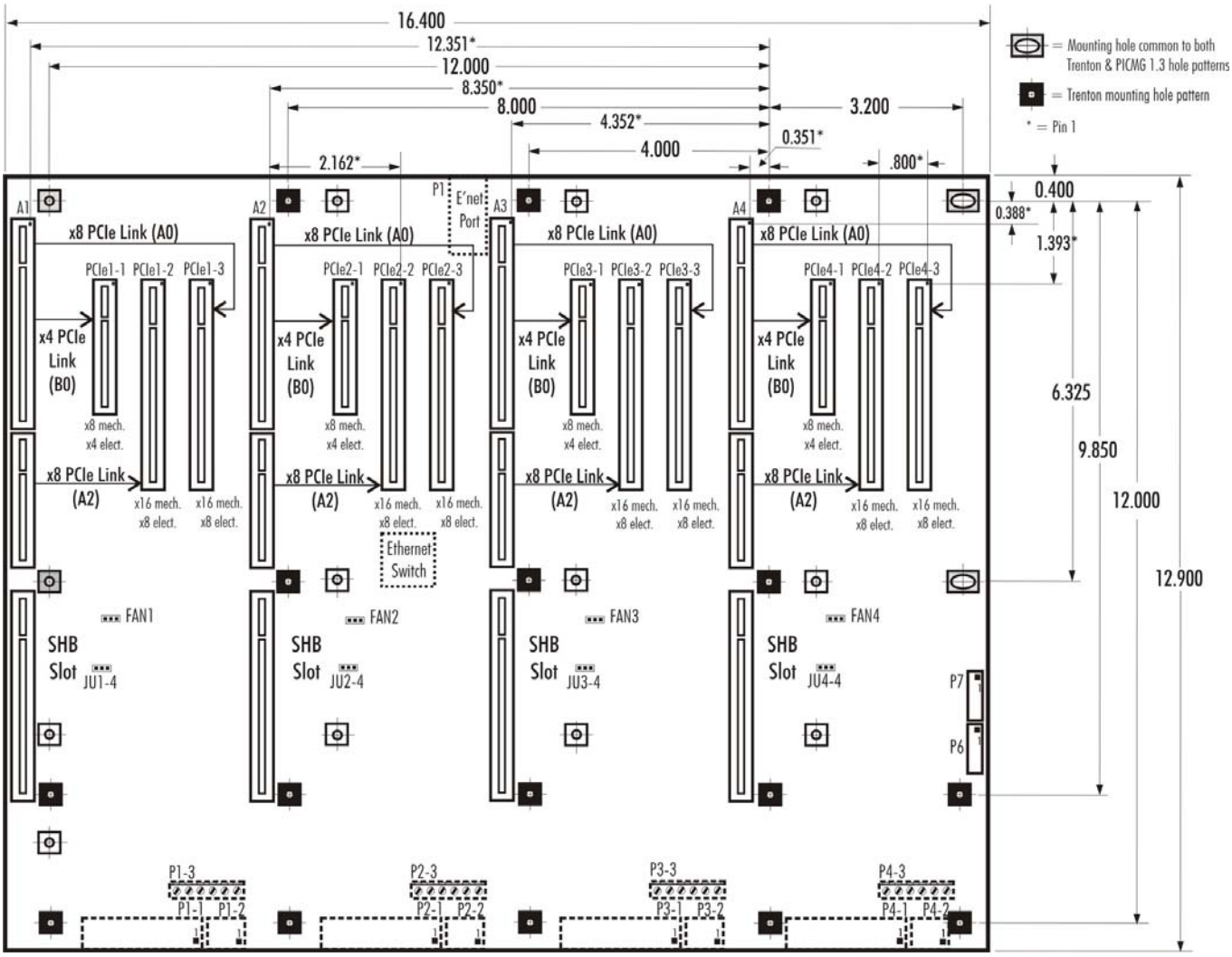
6890-000 BP4FS6890 DIMENSIONAL-DRAWING – SERVER-CLASS CONFIGURATION

Trenton Hole Pattern



6890-000 BP4FS6890 DIMENSIONAL-DRAWING – SERVER-CLASS CONFIGURATION

PICMG 1.3 Hole Pattern

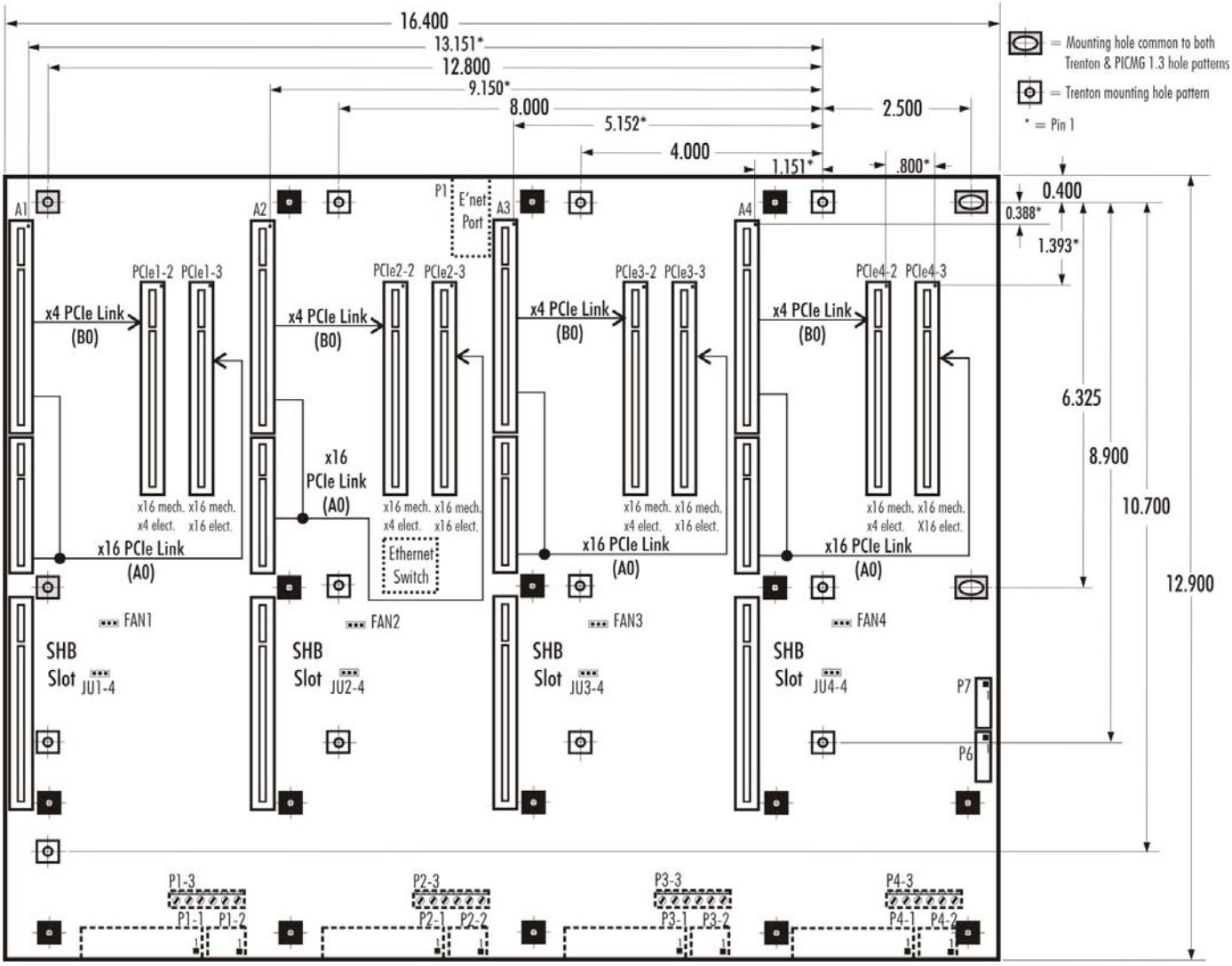


Notes:

- Dotted lines indicate connectors and other components that are populated based on model name and number. Refer to Backplane Configuration Table
- Typical PCIe connector centers are 0.049" from pin 1
- Mounting holes have a nominal 0.156" diameter
- Nominal PCB thickness: 0.080"
- All dimensions are inches.
- Suggested Trenton server-class PICMG 1.3 SHBs for use with the server-class BP4FS6890 backplane models:
    - Dual-processor SHBs: MCXT, MCXT-E, SLT and NLT
    - Single-processor SHBs: MCXI, SLI and NLI
    - Use MCX-series SHB if the backplane Ethernet fabric option is needed

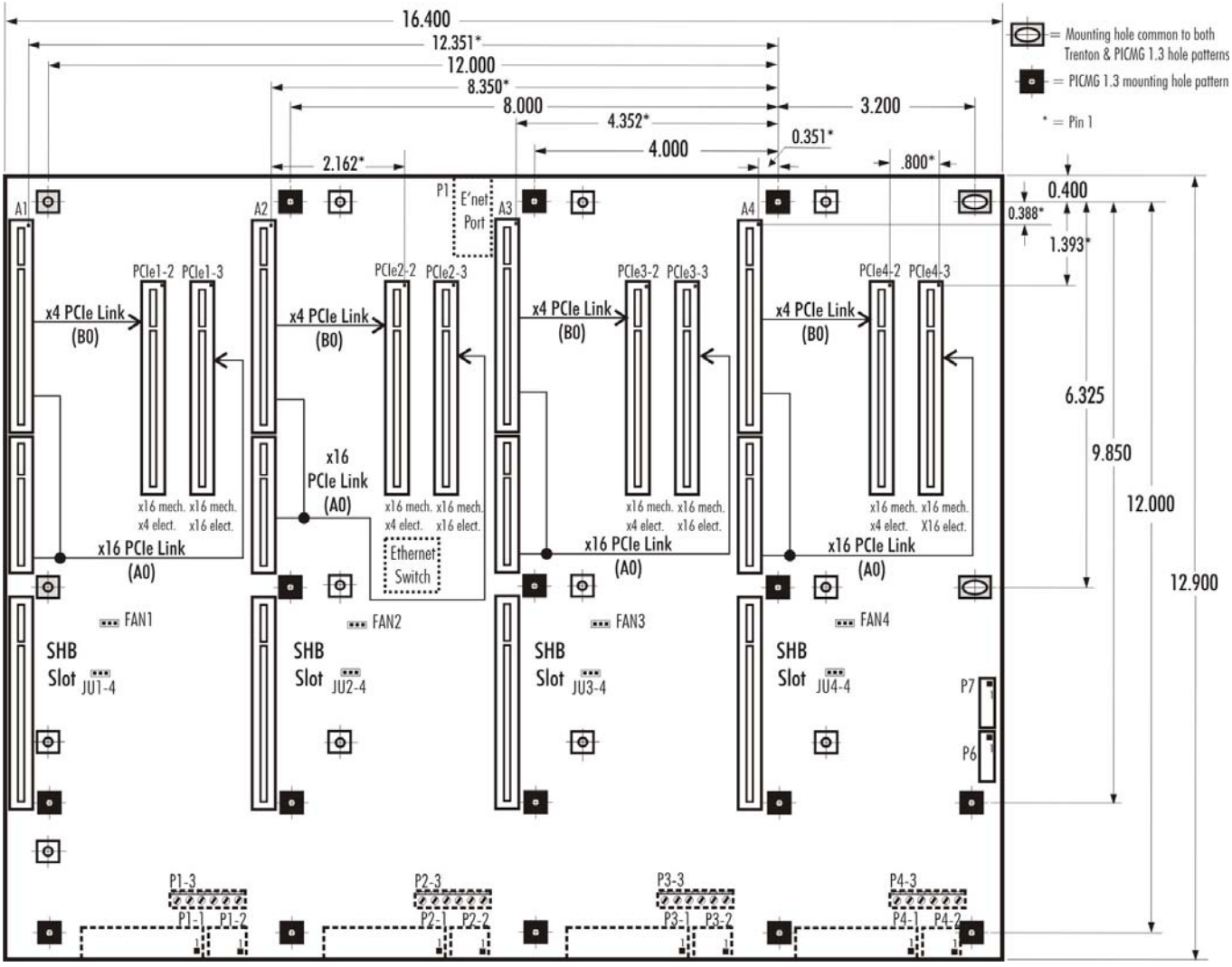
6890-000 BP4FS6890 DIMENSIONAL-DRAWING – GRAPHICS-CLASS CONFIGURATION

Trenton Hole Pattern



6890-000 BP4FS6890 DIMENSIONAL-DRAWING – GRAPHICS-CLASS CONFIGURATION

PICMG 1.3 Hole Pattern



Notes:

- Dotted lines indicate connectors and other components that are populated based on model name and number. Refer to Backplane Configuration Table
- Typical PCIe connector centers are 0.049" from pin 1
- Mounting holes have a nominal 0.156" diameter
- Nominal PCB thickness: 0.080"
- All dimensions are inches.
- Suggested Trenton graphics-class PICMG 1.3 SHBs for use with the server-class BP4FS6890 backplane models:
    - Dual-processor SHBs: MCGT, MCGT-E
    - Single-processor SHBs: MCGI, TQ9, TML and T4L
    - All Trenton graphics-class SHBs may be used if the backplane Ethernet fabric option is needed

6890-000 BP4FS6890 BACKPLANE CONFIGURATION TABLE

The BP4FS6890 four-segment PICMG 1.3 backplane can be factory-configured to operate with either PICMG 1.3 Graphics- or Server-class system host boards (SHBs). The model number column in the table below indicates the backplane's specific configuration. Server-class configurations must be matched to server-class SHBs and graphics-class configurations must be matched with graphics-class SHBs for optimum system performance.

Model#	Model Name & Type	SHB Connector D	ATX/EPS Connectors P1-1 P2-1 P3-1 P4-1	+12V Aux Connectors P1-2 P2-2 P3-2 P4-2	+12V Terminal Blocks P1-3 P2-3 P3-3 P4-3	Ethernet Hub and Port P1	PCIe slots per SHB segment
6890-005	BP4FS6890-SCSR, Server-class, Standalone, Right-angle ATX/EPS power connectors	No	Yes	Yes	No	No	2 – x16 mech. / x8 elect. 1 – x8 mech. / x4 elect.
6890-016	BP4FS6890-SCST, Server-class, Standalone, Terminal Block connectors	No	No	No	Yes	No	2 – x16 mech. / x8 elect. 1 – x8 mech. / x4 elect.
6890-025	BP4FS6890-SCER, Server-class, Ethernet, Right-angle ATX/EPS power connectors	No	Yes	Yes	No	Yes*	2 – x16 mech. / x8 elect. 1 – x8 mech. / x4 elect.
6890-036	BP4FS6890-SCET, Server-class, Ethernet, Terminal Block connectors	No	No	No	Yes	Yes*	2 – x16 mech. / x8 elect. 1 – x8 mech. / x4 elect.
6890-105	BP4FS6890-GC1SR, Graphics-class, Standalone, Right-angle ATX/EPS power connectors	No	Yes	Yes	No	No	2 – x16 mech. -- 1 x16 elect. & 1 x4 elect.
6890-116	BP4FS6890-GC1ST, Graphics-class, Standalone, Terminal Block connectors	No	No	No	Yes	No	2 – x16 mech. -- 1 x16 elect. & 1 x4 elect.
6890-125	BP4FS6890-GC1ER,Graphics-class, Ethernet, Right-angle ATX/EPS power connectors	No	Yes	Yes	No	Yes	2 – x16 mech. -- 1 x16 elect. & 1 x4 elect.
6890-136	BP4FS6890-GC1ET, Graphics-class, Ethernet, Terminal Block connectors	No	No	No	Yes	Yes	2 – x16 mech. -- 1 x16 elect. & 1 x4 elect.

*Trenton SLT/SLI and NLT/NLI system host boards do not support the Ethernet function on the backplane

CONFIGURATION JUMPERS

The setup of each SHB segment's configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post) in SHB segments, "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the SHB's I/O plate(s) at the top end of the backplane.

NOTE: JU4, 1-2 indicates the JU4 jumper in SHB segments one and two while JU4, 3-6 means the JU4 jumper in SHB segment three, four, five and six.

Jumper	Description
JU1-4, JU2-4, JU3-4, JU4-4	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. * Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies.

6890-000 BP4FS6890 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1-1, P2-1 **EPS Power Connector**
P3-1, P4-1 24 pin vertical dual row, Molex #44206-0007

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

P1-2, P2-2 **+12V Power Connector**
P3-2, P4-2 8 pin vertical dual row, Molex #44206-0005

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P1-3, P2-3 **Terminal Block Connector**
P3-3, P4-3 6 position terminal block, AMP, #796949-4
20 Amps per circuit

Pin	Signal
1	+12V
2	+12V
3	+12V
4	Gnd
5	Gnd
6	Gnd

P6 **PSON and SHB Reset Signal Connector**
16 pin dual row connector, 3M, #N2516-6002RB

Pin	Signal	Pin	Signal
1	PSON# - 1	2	Gnd - 1
3	PSON# - 2	4	Gnd - 2
5	PSON# - 3	6	Gnd - 3
7	PSON# - 4	8	Gnd - 4
9	SHB_RST - 1	10	Gnd - 1
11	SHB_RST - 2	12	Gnd - 2
13	SHB_RST - 3	14	Gnd - 3
15	SHB_RST - 4	16	Gnd - 4

6890-000 BP4FS6890 CONNECTORS (CONTINUED)

P7 **Power Button and Power Good Signal Connector**

16 pin dual row connector, 3M, #N2516-6002RB

Pin	Signal	Pin	Signal
1	PWRBT# - 1	2	Gnd - 1
3	PWRBT# - 2	4	Gnd - 2
5	PWRBT# - 3	6	Gnd - 3
7	PWRBT# - 4	8	Gnd - 4
9	PWRGD - 1	10	Gnd - 1
11	PWRGD - 2	12	Gnd - 2
13	PWRGD - 3	14	Gnd - 3
15	PWRGD - 4	16	Gnd - 4

P1 **10/100/1000 - Base-T Ethernet Connector – Backplane Hub Port (OPTIONAL)**

8 pin right angle shielded RJ-45 connector, Pulse, #J0035D21BNL

Pin	Signal
1	RXD-
2	RXD+
3	RCI
4	RC
5	TC
6	TCI
7	TXD-
8	TXD+

FAN1 **Available System Cooling Fan Power Connector**
FAN2 Standard 3 pin cooling fan power header
FAN3
FAN4

Pin	Signal
1	Gnd
2	+12V
3	NC

This page intentionally left blank.

Chapter 6 - 2U Butterfly Backplanes

6741-000 BPG6741

The BPG6741 is a graphics-class PICMG-compatible backplane which is a six-layer .062" thick PCB. It supports PICMG® 1.3 compliant SHBs and the butterfly form factor is designed for use in 2U chassis.

The backplane has one PCI Express® slot which accepts an SHB Express™ system host board (SHB). It also has three Express slots (PCIe1, PCIe3 and PCIe4) which provide the mechanical connections between the PCI Express option cards and the SHB.

PCIe1 and PCIe3 option card slots are located on side B of the 6741. Side B is opposite the SHB and Side B slots are driven by x1 PCI Express electrical links from a Trenton MCX-series SHB. PCIe4 is a x16 mechancial slot located on Side A of the butterfly backplane and is driven by x16 PCI Express electrical link from a graphics-class SHB. It is capable of supporting high-end PCI Express video and graphics cards.

The audio controller on the BPG6741 backplane eliminates the need to dedicate an option card slot to a sound card. The USB audio controller supports a variety of speaker, headset and microphone configurations. The USB4 port from the Trenton MCG-series SHB provides the input for the USB audio controller and the USB4 input becomes Audio0 on the BPG6741 backplane.

The BPG6741 supports the optional Ethernet routing feature of the SHB Express specification. The Ethernet version of the BPG6741 provides one 10/100/1000Base-T Ethernet RJ-45 connector on side B of the butterfly backplane. The required Ethernet connector location may necessitate a mechanical modification to the chassis in order to facilitate proper backplane mounting within the enclosure. It also has one USB 2.0 header which is capable of supporting up to two USB 2.0 general purpose I/O ports on the backplane.

Audio, USB and Ethernet functionality on the BPG6741 is dependent on the SHB providing the I/O capability to edge connector C of the backplane. In order to take advantage of these optional I/O features, the SHB in the system must be able to support the connections as specified in the PCI Industrial Manufacturers Group's *SHB Express™ System Host Board PCI Express Specification, PICMG® 1.3*.

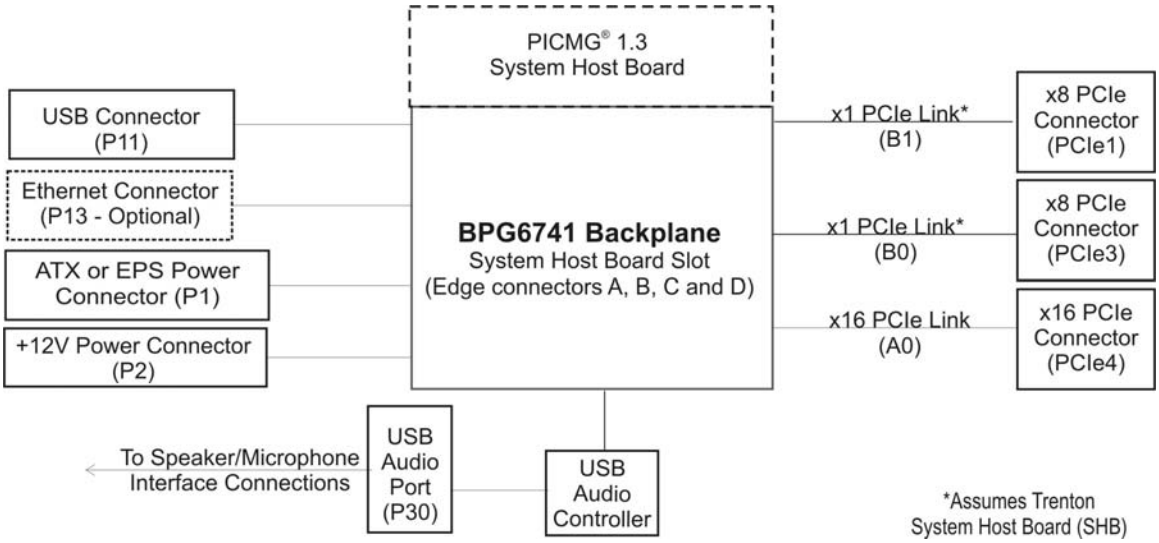
The standard BPG6741 backplane is available with a low-profile right-angle power connector suitable for use with either an ATX or EPS power supply

---

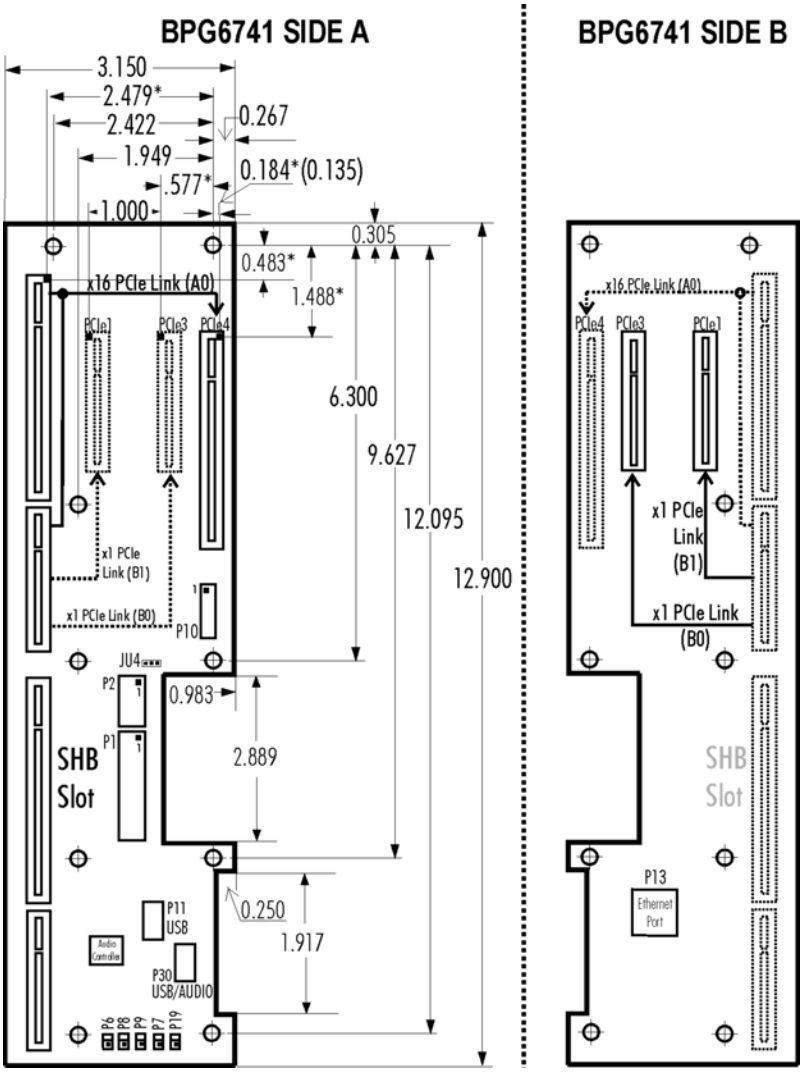
CAUTION: In some ATX/EPS systems, the power may appear to be off while the +5VSB signal is still present and supplying power to the SHB, option cards and other system components. The +5VAUX LED on a Trenton PICMG 1.3 backplane monitors the +5VSB power signal; "green" indicates that the +5VSB signal is present. Trenton backplane LEDs monitor all DC power signals, and all of the LEDs should be off before adding or removing components. Removing boards under power may result in system damage.

Models with other power configurations may be available. Contact Trenton Technology for more information.

6741-000 BPG6741 BLOCK DIAGRAM



6741-000 BPG6741 BLOCK DIAGRAM



CONFIGURATION JUMPER

The setup of the configuration jumper on the backplane is described below. * indicates the default value of the jumper.

NOTE: For the two-position jumper (3-post), "RIGHT" and "LEFT" refer to positioning when the backplane is viewed with the slots at the top end of the backplane.

Jumper	Description
JU4	**+5V Auxiliary Voltage** Install on the LEFT if +5V auxiliary voltage is provided by the standard +5V supply. This option is used for systems which do not have either an ATX or EPS standard power input. This mode provides the necessary +5V for the SHB's +5VAUX signal lines. Sleep mode recovery is not supported using non-ATX/EPS power supplies. Install on the RIGHT if +5V auxiliary voltage is provided by a separate +5VAUX signal input pin. This enables the necessary SHB power signaling and allows recovery from sleep mode. This option is used for ATX or EPS standard power supplies. *

6741-000 BPG6741 CONNECTORS

NOTE: Pin 1 on the connectors is indicated by the square pad on the PCB.

P1 - ATX/EPS Power Connector

24 pin right angle dual row, Molex #39-30-1240

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	Gnd	15	Gnd
4	+5V	16	PSON#
5	Gnd	17	Gnd
6	+5V	18	Gnd
7	Gnd	19	Gnd
8	PWRGD	20	-5V
9	+5VAUX	21	+5V
10	+12V	22	+5V
11	+12V	23	+5V
12	+3.3V	24	Gnd

6741-000 BPG6741 CONNECTORS (CONTINUED)

P2 - +12V Power Connector

8 pin right angle dual row, Molex #39-30-0080

Pin	Signal	Pin	Signal
1	Gnd	5	+12V
2	Gnd	6	+12V
3	Gnd	7	+12V
4	Gnd	8	+12V

P6 - Power-On Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PSON#
2	Gnd

P7 - Power Button Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRBT#
2	Gnd

P8 - Reset Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SHB_RST#
2	Gnd

P9 - Power Good Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	PWRGD
2	Gnd

6741-000 BPG6741 CONNECTORS (CONTINUED)

P10 - I/O Power Connector

20 pin right angle dual row header, Molex #87833-2020

Pin	Signal	Pin	Signal
1	Gnd	2	+12V
3	IPMB_DA	4	Gnd
5	IPMB_CL	6	+5V
7	SMDAT	8	+5VAUX
9	SMCLK	10	+3.3V
11	PWRBT#	12	PSON#
13	Gnd	14	SHB_RST#
15	PWRGD	16	5VAUX
17	GND	18	5VAUX
19	GND	20	-12V

P11 - Universal Serial Bus (USB) Connector

10 pin right angle dual row header, 3M, #N2510-5002UB (+5V fused with self-resetting fuses)

Pin	Signal	Pin	Signal
1	+5V-USB0	2	+5V-USB1
3	USB0-	4	USB1-
5	USB0+	6	USB1+
7	Gnd-USB0	8	Gnd-USB1
9	Chassis Gnd	10	Chassis Gnd

P13 - 10/100/1000Base-T Ethernet Connector - LAN 0 (Optional)

8 pin right angle shielded RJ-45 connector, Molex #43860-0025

Pin	Signal
1	TRP1+
2	TRP1-
3	TRP2+
4	TRP3+
5	TRP3-
6	TRP2-
7	TRP4+
8	TRP4-

P19 - SMBUS Connector

2 pin right angle single row header, Molex #22-05-3021

Pin	Signal
1	SMBUS
2	Gnd

6741-000 BPG6741 CONNECTORS (CONTINUED)

P30 - Universal Serial Bus (USB) Audio Connector

10 pin right angle dual row header, 3M, #N2510-5002UB

Pin	Signal	Pin	Signal
1	LineIn Lt.	2	LineIn Rt.
3	Gnd	4	Gnd
5	Mic P	6	Mic In
7	Gnd	8	Gnd
9	Linout Lt.	10	LineOut Rt.